Wide-Dynamic-Range Continuous-Time ∆Σ A/D Converter for Low-Power Energy-Scavenging Applications

by

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Claudia Gunsch

Dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy in the Department of Electrical and Computer Engineering in the Graduate School of Duke University 2011
ABSTRACT

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Abstract

Many medical, environmental, and industrial control applications rely on wide-dynamic-range sensors and A/D converter systems. For most photo-detector-based applications, the input-current is integrated onto a capacitor, either with a variable time, or a variable capacitor value, followed by a sample-and-hold and a voltage A/D converter. The penalty for achieving wide-dynamic-range with the above approach is power and circuit complexity.

We propose to use the unique properties of current-input continuous-time ΔΣ A/D converters to combine the photo-detector current-integration with simultaneous wide-dynamic-range A/D conversion, using programmable reference currents and programmable clock frequencies.

A programmable current-input wide-dynamic-range ΔΣ A/D converter is designed and fabricated using MOSIS AMI 1.5 µm 5 V CMOS process. The programmable A/D converter test results exhibit a consistent 12-bit resolution over the programmability range of the reference-currents, from 17.2 nA to 4.4 µA. The supply-current varies from 60 µA to 240 µA, whereas the A/D converter sample-rates increase from 4 Samples/s to 1 kSamples/s, achieving an overall system-dynamic-range of 20-bits.

An RF-powered version is designed and fabricated using MOSIS ON 0.5 µm 3 V CMOS process. It is designed to work at 128 Samples/s to 11.25 kSamples/s
sample-rates, achieving 12-bit resolution with only 128 oversampling ratio. The A/D converter supply-current is designed to range from 10 µA to 70 µA to allow its integration with an RF-power source. The RF-powered version of the programmable ΔΣ A/D converter includes an on-chip voltage regulator that generates a stable 3 V DC-voltage, and consumes only 15 µA current.
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List of Abbreviations and Symbols

Symbols

Put general notes about symbol usage in text here. Notice this text is double-spaced, as required.

\[ \Omega \] Discrete-time frequency.

Abbreviations

BJT Bipolar junction transistor.
CIFF Cascade of integrators with feed-forward.
CIFB Cascade of integrators with feedback.
CMOS Complementary metal-oxide semiconductor.
CTAT Complementary to the absolute temperature.
DNL Differential non-linearity.
INL Integral non-linearity.
ENOB Effective number of bits.
FFT Fast Fourier transform.
NBW Noise bandwidth.
NTF Noise transfer function.
OSR Oversampling ratio.
PD Photo-detector
PTAT Proportional to the absolute temperature.
PTV  Process, temperature, supply-voltage.
RF   Radio-frequency.
RFID Radio-frequency identification.
SNR  Signal to noise ratio.
STF  Signal transfer function.
THD  Total harmonic distortion.
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disappoint me and works! And last but not least I would like to thank my friends Heather Wake, Matt Royal, Ritika Singh, Sabarni Palit, Sulochana Dhar and Xin Cai for interesting discussions, ideas, company and just plain fun time at Duke!
Wide-dynamic-range imaging-sensors are necessary to capture high-contrast images. Wide-dynamic-range current-sensing is achieved by integrating the current onto a capacitor. Commercial current-input A/D converters rely on this principle, using transimpedance-amplifier integrators, $G_m - C$, with variable-size capacitors, to increase the dynamic-range of the A/D conversion.

Biomedical-sensors, that capture low-level voltage signals, use programmable-gain amplifiers to increase the signal-to-noise ratio and to match the signal to the A/D converter input to achieve high signal-to-noise ratio (SNR). In both cases, an additional level of circuit complexity is required between the sensor and the A/D converter, thus considerably increasing the power consumption and the complexity of the overall system.

In this dissertation, we propose to build a programmable, wide-dynamic-range A/D converter using inherent characteristics of the current-input continuous-time ΔΣ A/D converter. The complexity of the current-sensing A/D converter is signifi-
cantly reduced if the input-current can be applied directly to the $\Delta \Sigma$ A/D converter. We propose to increase the dynamic-range through programmable clock-frequencies and programmable reference-currents of the continuous-time $\Delta \Sigma$ A/D converter. At small input-current levels, the proposed programmable $\Delta \Sigma$ A/D converter achieves a significantly higher accuracy than at high input-current levels. Power consumption is also significantly reduced at low input-current levels, due to the accompanying low reference-currents and slow clock-frequencies. The proposed programmable continuous-time $\Delta \Sigma$ A/D converter achieves a consistent 10-12 bits of resolution over the programmability range of the input-current, and at low input-current levels the A/D converter performance is comparable to that of an ideal 20-bit resolution A/D converter. Because it is assumed that many bio-medical applications require high-resolution A/D conversion at only low-level input currents, the proposed system is a power-efficient alternative to the traditional high-resolution A/D converters.

With the development of radio-frequency-identification (RFID) systems and wireless sensor-networks, a new approach to integrating wireless-sensors with RFID technology is becoming practical in medical and environmental monitoring areas. In such applications, the most important property of a sensor A/D converter is its low-power consumption and the ability to detect small-signals without power-penalty. The proposed programmable $\Delta \Sigma$ A/D converter can meet such requirements. Continuous-time $\Delta \Sigma$ A/D converter architecture, additionally, allows for easy data-communication from the A/D converter output to an external reader due to its serial nature.

In this dissertation, we also propose combining the programmable $\Delta \Sigma$ A/D converter with an RF-power source. The serial single-bit nature of the $\Delta \Sigma$ A/D converter output allows it to be efficiently backscatter-transmitted to the reader.
Current-input ΔΣ A/D converters can be used in any photo-detector-based sensor applications. Biomedical and chemical sensors, e.g. colorimetric, fluorescent, and interferometric, as well as all imaging-sensors, use photo-detectors and light-emitting diodes as signal detectors. Colorimetric sensors sense a change in color after a chemical reaction takes place [48, 36]. Fluorescent sensors rely on fluorescent probes that exhibit selectivity for certain metals, or fluorophore binding to certain components [22, 28]. Interferometric sensors employ waveguide structures to measure phase shifts [13, 9]. Detector arrays usually require low-power, low-cost, and small-area CMOS reverse-biased photo-detectors [17]. Another advantage of CMOS photo-detectors is that they can be integrated on the same chip as the A/D converter and the signal-processing electronics. Photo-detector-current measurements and/or analog-digital conversion methods can vary from single-slope integration and averaging [43] to ΔΣ modulation [27]. Wide-dynamic-range A/D converters are required for biomedical and chemical-sensor applications, where the input-current levels are low and the sensor areas are small. Photo-detector current-integration has its limitations. Maximum signal-to-noise-ratio (SNR) is limited by the integration time, 1/f noise, and photo-detector shot noise.

Low-power applications, e.g. portable medical equipment, medical implants, and wireless sensors, require low-power A/D converters. Remote-sensor networks based on operating systems, such as Tiny-OS, allow for multiple-sensors, e.g. temperature, humidity, acceleration, vibration, sound and atmospheric effects, to be integrated in a single system [14]. Low-power operation of the sensor is critical for the system to operate on battery, solar, RF or vibration-power sources. Successive-approximation-register (SAR) A/D converters are successfully employed in wireless sensor-nodes [40]. Medical implants with integrated A/D converters, digital-signal processing, and amplifiers rely on batteries or transcutaneous links for power transfer, and, in
general, use low-power switched-capacitor $\Delta\Sigma$ A/D converters [49]. Medical sensors and data-acquisition systems rely on $\Delta\Sigma$ A/D converters for their high-resolution and low-noise measurements. Successive-approximation-register (SAR) A/D converter architectures are more sensitive to noise, whereas $\Delta\Sigma$ A/D converters have an excellent differential non-linearity (DNL) and better noise-erformance [42]. Continuous-time $\Delta\Sigma$ A/D converters with 12-bits resolution, for low-power battery-powered medical devices, were reported in [18].

For current-input signals, successive approximation register (SAR) A/D converters will require low-noise and low-power sample-and-hold circuits [47]. Successive-approximation-register (SAR) A/D converter architectures are based on switched-capacitor and charge-sharing digital-to-analog (D/A) converters that are low-power but have large areas due to their array of capacitors. Also careful capacitor matching is required to achieve a wide-dynamic-range. State-of-the-art successive-approximation-register A/D converters, made by Texas Instruments, have 16-bits resolutions at speeds of 4 MSamples/s. Successive-approximation-register A/D converters can also be flexible. Because SAR A/D conversion is based on a binary search algorithm the resolution of the A/D converter is controlled by the number of binary-comparisons [35]. By controlling the number of binary-comparisons and therefore the conversion-time, with a reconfigurable comparator, a 12-bit to 8-bit power-efficient A/D converter was realized in [40]. Successive-approximation-register A/D converters can monitor the input-signal-level with low-power, an important property for sensor data-monitoring and fault-detection [2]. The lowest-power successive-approximation-register A/D converter, operating with only 1 $\mu$W power, and fabricated in 0.18 $\mu$m CMOS is demonstrated in [33].
Low-Power and Wide-Dynamic-Range A/D Converters

Wireless sensor-networks, as well as portable medical-applications require low-power A/D converters to be battery-operated, or in the case of the radio-frequency-identification (RFID) passive-tags to be RF-powered. The two of the most prevalent low-power and medium-to-high resolution converters are successive-approximation-register (SAR) and $\Delta\Sigma$ A/D converters.

Low-power applications can, in-principle, be combined with imaging, bio-medical, environmental, and process control applications that require high-resolution A/D converters to accurately measure low-level signals. High-resolution A/D converters consume a lot of power, whereas integrating the sensor with a programmable-gain-amplifier and a medium-resolution A/D converter also increases the power penalty and the complexity of the system.

Integrating high-resolution and wide-dynamic-range A/D converters in a battery-powered or RF-powered application can be challenging, due to high-resolution A/D
converters’ significant power requirements. We propose to achieve a low-power and wide-dynamic-range A/D converter by integrating the programmable-gain amplifier with the A/D converter. Continuous-time $\Delta \Sigma$ A/D converters are well suited for such an approach. Programmable dynamic-range-low-power continuous-time $\Delta \Sigma$ A/D converters, combined with a low-power programmable current-controlled ring-oscillators, are ideal candidates for battery-powered and RF/solar/vibration-powered photo-detector-based sensor-applications.

2.1 Low Power A/D Converters

Continuous-time $\Delta \Sigma$ A/D converter architectures are not new, and their applications in low-power A/D converters are well established [39]. Continuous-time $\Delta \Sigma$ A/D converters are inherently low-power, as in the example of a 3-rd order low-power RC-integrator-based converter that achieves 80 dB signal-to-noise dynamic range (SNDR) with only 135 $\mu$W of power consumption and 1.5 V supply voltage [18]. One of the fist $\Delta \Sigma$ A/D converters was built as a continuous-time and incremental $\Delta \Sigma$ [32]. It achieved a 15-bit absolute accuracy with a 1 s conversion time and 65 $\mu$W power. They showed that by increasing the number of clock cycles per conversion, it is possible to improve the resolution, but not the accuracy of the A/D conversion. The accuracy of the $\Delta \Sigma$ A/D converter is limited due to input-deadzones around which the quantization error does not decrease with the number of clock cycles [32]. It achieved a 16-bit resolution with only 362 clock-cycles, using a second-order $\Delta \Sigma$ modulator. Another example is a design in 0.5 $\mu$m process that achieves a 12-bit resolution while consuming only 90 $\mu$A supply-current at 1.5 V supply-voltage [18].

As shown in [18], there is a trade-off between $\Delta \Sigma$ A/D converter order, dynamic-range, and its power consumption. Higher order $\Delta \Sigma$ modulators are faster, using less clock cycles per sample, but require more amplifiers and more sophisticated digital
output-filtering, thus increasing the A/D conversion-power [18].

2.2 Programmable and Wide Dynamic Range A/D Converters

For current-input applications, one of the most prevalent methods for achieving a wide-dynamic-range A/D conversion is the current-integration method, with a variable capacitor or a variable time, together with a fixed resolution voltage-input A/D converter, as shown in Fig. 2.1. Many commercial current-input A/D converters, such as Texas Instruments 'DDC118 Octal Current-Input 20-Bit Analog-to-Digital Converter' and Analog Devices 'ADAS1128 128-Channel 24-Bit Current-to-Digital ADC', use this method.

The benefits of integrating the light onto a capacitor are significant in improving the signal-to-noise ratio [44]. The current-integration increases the noise-power linearly with time, whereas the signal-power is increasing quadratically. The trade-off in such a scheme is that having large integration-capacitors for given integration-times allow us to measure large currents, but small-currents integrate to small voltages, that are lost in the voltage readout-noise. In opposite, small integration-capacitors for given integration-times allow us to have large-gains for small input-currents, but

Fig. 2.1. Current A/D converter with transimpedance amplifier.
large-currents integrate only up to a fixed saturation-voltage of the capacitor. Additionally, using transimpedance amplifiers increases the A/D conversion circuit-complexity and power-consumption.

In voltage-input applications, to achieve a wide-dynamic-range A/D conversion, the general approach is to include a programmable-gain amplifier before a fixed-resolution voltage-input A/D converter as shown in Fig. 2.2.

Most commercial A/D converters achieve wide-dynamic-ranges by using programmable-gain amplifiers (PGA). Programmable-gain amplifiers decrease the input-voltage range, but because the least-significant-bit (LSB) size also decreases, the system dynamic-range increases, as shown in Fig. 2.3.

Another important method in improving the A/D converter dynamic range, is the voltage-reference scaling [5]. If we assume that the A/D converter accuracy is mostly determined by the least-significant-bit (LSB) value, then decreasing the voltage reference and maintaining the resolution will decrease the LSB value and, therefore, increase the A/D conversion accuracy. Decreasing the reference voltage effectively increases the signal-to-quantization-noise ratio (SQNR). Many A/D converters are

![Fig. 2.2. Voltage A/D converter with programmable gain amplifier.](image-url)
claimed to have an increased dynamic range by comparing the LSB achieved with a small reference voltage to that achieved with large reference voltage. Assuming the A/D converter has a 12-bit resolution, then for reference voltage of $V_{ref1} = 5\, V$ the least-significant-bit (LSB) is

$$LSB_1 = \frac{5}{2^{12}} = 1.22\, mV,$$

and for $V_{ref2} = 0.1\, V$, it is

$$LSB_2 = \frac{0.1}{2^{12}} = 24.4\, \mu V.$$

Thus, this two-state programmable A/D converter effective resolution, $R_{eff}$, is given by
\[ R_{eff} = \log_2(5000/0.0244) = 17.6 \text{ bits}. \]

Programmable-gain amplifier method, to achieve wide dynamic range A/D converter, is almost identical to voltage-reference scaling method. The only significant difference is that in programmable-gain amplifier method the amplifier’s internal noise limits the achievable dynamic range, while for voltage-reference scaling method input-buffer internal noise plays an important role. In programmable-gain amplifiers, the signal is amplified with an additive noise, but the voltage or current-references are left constant [3].

Another approach to increase the dynamic range of A/D converter is software bit-shifting. Software bit-shifting method introduces a signal gain. But unlike the programmable-gain amplifier method, the dynamic range of the A/D converter with \( \mu \)P (microprocessor) implemented digital-output bit-shifting decreases the dynamic range [4]. In a software bit-shifting method, the final A/D conversion results are shifted to the left by one and a zero is added to the right (e.g. \([10111001] \rightarrow [01110010]\)). Software bit-shifting increases the LSB size by a factor of 2, and because the maximum analog-input value does not change with the digital-output bit-shifting, the dynamic range decreases by a factor of 2. This concept is illustrated in Fig. 2.4.

Unlike conventional A/D converters, \( \Delta \Sigma \) A/D converters have an additional parameter, the oversampling ratio (OSR), that can be programmed to achieve a wide dynamic range A/D conversion. \( \Delta \Sigma \) A/D converter system diagram is shown in Fig. 2.5. Programmable-oversampling method for \( \Delta \Sigma \) A/D converters is equivalent to programmable-gain method with the additional benefit of input-signal gain. Increasing the oversampling ratio improves the signal-to-quantization-noise ratio (SQNR)
and, therefore, it improves the resolution and the number of bits.

In an ideal second-order modulator, doubling the OSR increases the SQNR by a factor of $2^5 = 32$ or 15 dB, and increases the resolution by 2.2 bits [34, 38]. In an ideal first-order modulator, doubling the OSR increases the SQNR by a factor of $2^3 = 8$ or 9 dB, and increases the resolution by 1.2 bits. Increasing the OSR is similar to programmable gain with one significant difference. Increasing the OSR lowers the
quantization noise for a given input-signal level, therefore increasing the dynamic
range [34]. Many commercial ΔΣ A/D converters allow choosing the oversampling
ratio. Texas Instruments '24-Bit Analog-to-Digital Converter' achieves high resolu-
tions with programmable-gain amplifier and programmable-OSR ΔΣ A/D converter,
where the programmable-gain amplifier is a discrete-time switched-capacitor-based
integrator.

2.3 RF-Powered Sensors

Wireless-battery-powered sensors, and RF/Solar/Vibration-powered sensors re-
quire low-power A/D converters to be integrated on-chip. The challenge is designing
a low-power wide-dynamic-range A/D converter, that can be programmed to match
the changing environmental conditions.

An radio-frequency-identification (RFID) chip for biomedical-applications, includ-
ing a temperature-sensor, working in the industrial-scientific-medical (ISM) band of
13.56 MHz is reported in [10]. Another RFID tag with integrated photo-sensor is
demonstrated in [12]. To increase the data-rate, ISM band of 915 Mhz is used. A
temperature and gas sensor RFID tag is reported in [21]. The tag consumes 3 µA in
the gas-measurement mode, and 12 µA in the temperature-measurement mode.

Another critical component for successful integration of sensors and A/D con-
verters in RFID tags is the RF-power rectifier. The rectifier efficiency determines
the range of the passive-tag operation. Methods to design an optimum-performance
rectifiers are discussed in [45, 15].
2.4 Programmable Continuous-Time $\Delta\Sigma$ A/D Converters

In this section, the application of a low-power continuous-time $\Delta\Sigma$ A/D converter in the context of a programmable wide-dynamic-range is discussed. Our proposed method of using a continuous-time $\Delta\Sigma$ A/D converter for simultaneous current-integration and current-input A/D conversion allows us to achieve a wide-dynamic-range, low-power, a programmable input-current-range, and a low circuit-complexity. Also the inherent anti-aliasing filter of the continuous-time $\Delta\Sigma$ A/D converter filters the shot noise of the photo-detector.

2.4.1 Programmable Wide-Dynamic-Range

A continuous-time $\Delta\Sigma$ A/D converter with programmable reference-currents and programmable clock-frequency is proposed. Its staircase transfer function is shown in Fig. 2.6 and Fig. 2.7.

Fig. 2.6. Programmable $\Delta\Sigma$ A/D converter staircase transfer-function.
Programmability of the $\Delta \Sigma$ A/D converter is very similar to programmable gain amplifier (PGA) approach, as well as programmable reference voltage (or current) approach discussed earlier. A significant difference in programming $\Delta \Sigma$ A/D converter directly is allowing the circuit to operate with reference currents that correspond that correlate with input signal, therefore saving valuable power. The tradeoff is the conversion time will increase with lower reference-currents and therefore the total energy-per-sample will be the same or more.

2.4.2 Continuous-Time Second-Order $\Delta \Sigma$ A/D Converter

Continuous-time $\Delta \Sigma$ A/D converters are, in general, designed based on a discrete-time $\Delta \Sigma$ modulator model [34]. Discrete-time $\Delta \Sigma$ modulators are easily modeled due to the digital nature of their noise-transfer-functions (NTF) and signal-transfer-
functions (STF). In discrete-time $\Delta \Sigma$ modulators, the NTF and STF are, simply, two digital filters: NTF - highpass filter, STF - lowpass filter. In contrast, the STF and the NTF of the continuous-time $\Delta \Sigma$ modulators are not as easily defined, because the data-representation, in the modulator, changes from a continuous-time to a discrete-time, and back. One possible representation of a discrete-time $\Delta \Sigma$ modulator is shown in Fig. 2.8, and is based on a cascade of delayed-integrators with feedback (CIFB) architecture [34]. For this particular architecture of a discrete-time $\Delta \Sigma$ modulator, the STF and NTF digital-filters are calculated and optimized based on two feedback coefficients, $a_1$ and $a_2$.

![Fig. 2.8. Second-order CIFB discrete-time $\Delta \Sigma$ A/D converter model.](image)

Once the model discrete-time $\Delta \Sigma$ modulator feedback coefficients, $a_1$ and $a_2$, and the noise-transfer-function (NTF) $z$-transforms are determined, an equivalent continuous-time $\Delta \Sigma$ modulator parameters can be estimated. Two $\Delta \Sigma$ modulators, continuous-time and discrete-time, are considered to be equivalent if the loop impulse responses from the output of the quantizer to the input of the quantizer, at the sampling instances, are equal. The transformation between a continuous-time and a discrete-time filters is called an impulse-invariant transformation [29]. Continuous-time $\Delta \Sigma$ circuit implementation diagram is shown in Fig. 2.9.
The loop-filter transfer-function of the discrete-time ΔΣ modulator, \( LF_d(z) \), and its impulse-invariant-equivalent continuous-time transfer function, \( LF_d(s) \), are given by

\[
LF_d(z) = \frac{a_1}{(z - 1)^2} + \frac{a_2}{z - 1},
\]

(2.1)

and

\[
LF_d(s) = \frac{a_1(1 - (sT_s)/2)}{(sT_s)^2} + \frac{a_2}{sT_s} = \frac{a_1 + sT_s(a2 - a1/2)}{(sT_s)^2},
\]

(2.2)

respectively, where \( T_s \) is the clock period, \( a_1 \) and \( a_2 \) are the feedback-coefficients of the discrete-time ΔΣ modulator. The loop-filter transfer-function of the continuous-time second-order ΔΣ schematic model, \( LF_{sch}(s) \), is given by

\[
LF_{sch}(s) = \frac{i_1 G_m}{s^2 C_1 C_2} + \frac{i_1}{sC_2} = \frac{i_1 G_m + sC_1 i_2}{s^2 C_1 C_2},
\]

(2.3)

where \( i_1 \) and \( i_2 \) are the reference currents, \( C_1 \) and \( C_2 \) are the integration-capacitor values, and \( G_m \) is the transconductance of the amplifier. By equating the coefficients of \( LF_c(s) \) and \( LF_d(s) \), the continuous-time ΔΣ schematic model parameters, \( F_s, i_1, i_2, C_1, C_2, G_m \), can be estimated with one of the following sets of equations.
\[ G_{m1} = F_s C_1, \]  
\[ i_1 = F_s C_2 a_1, \]  
\[ i_2 = F_s C_2 (a_2 - \frac{a_1}{2}), \]

or,

\[ G_{m1} = \frac{a_1}{i_1} C_1 C_2 F_s^2, \]  
\[ i_2 = C_2 (a_2 - \frac{a_1}{2}) F_s, \]

where \( F_s \) is the clock frequency. There are three independent equations in the first set, and only two in the second set. In both cases there are six independent variables, \( F_s, i_1, i_2, C_1, C_2, \) and \( G_{m1}. \) The first set of equations is used when \( F_s, C_1, \) and \( C_2 \) variables are fixed by the application, and the second set of equations when \( F_s, i_1, C_1, \) and \( C_2 \) variables are fixed.

For the given reference-current, \( i_1, \) fixed by the application, to minimize the power-consumption of the A/D converter, the clock-frequency, \( F_s, \) and the transconductance of the amplifier, \( G_{m1}, \) must be minimized simultaneously. The tradeoff is that, decreasing clock-frequencies and for a fixed input-current, the value and the size of the first integrating-capacitor increases. The integrating-capacitor size is, ultimately, constraint by the chip area. For the given integrating-capacitor values, \( C_1 \) and \( C_2, \) and the reference-currents, \( i_1 \) and \( i_2, \) the A/D converter clock frequency, \( F_s, \) and the transconductance of the amplifier, \( G_{m1}, \) are uniquely determined, thus setting the minimum-power of the A/D converter.
The discrete-time $\Delta \Sigma$ modulator design starts with designing and optimizing the noise-transfer-function (NTF) highpass filter. The designed discrete-time, highpass filter is Chebyshev II filter with a corner frequency of $W_n = \pi/256$ rad/s and the filter attenuation in the stopband of $R = 80$ dB. Highpass noise-transfer-function (NTF) and the corresponding feedback coefficients are given by

$$NTF(z) = \frac{z^2 - 2z + 1}{z^2 - 0.901z + 0.3189}, \quad (2.6)$$

and,

$$a_1 = 0.4179, \quad (2.7)$$
$$a_2 = 1.0990,$$

respectively.

NTF pole-zero and highpass-filter transfer-function plots are shown in Fig. 2.10 and Fig. 2.11, respectively. NTF zeros at $z = 1$ are the result of the integrators in the loop and are fixed for the cascade-of-feedback-integrators (CIFB) $\Delta \Sigma$ architecture. Whereas, the NTF poles are determined by the feedback coefficients, $a_1$ and $a_2$. Pole placement determines the effectiveness of the NTF zeros at DC, at $z = 1$, as well as NTF gain at high frequencies, at $z = -1$. Placing poles too close to $z = 1$, lowers the effectiveness of zeros at $z = 1$, and lowers the signal-to-noise ratio. Placing poles too far from $z = 1$, increases the out-of-band gain of the NTF, and compromises the stability of the $\Delta \Sigma$ modulator. For a second-order $\Delta \Sigma$ modulator to be stable, Lee’s criterion requires that the out-of-band gain of the noise transfer function (NTF) be limited to $1.5$ [34, 11]. The placement of zeros and the out-of-band gain of NTF are more important than the placement of poles [34]. This particular design is a bit
aggressive, placing the poles far from the zeros, thus, achieving a good-quantization noise suppression at the expense of the limited input-range, and instability when the value of the input-current becomes nearly equal to the reference currents.

Fig. 2.10. Second-order Chebyshev II high-pass filter pole-zero.

Given the continuous-time $\Delta \Sigma$ A/D converter parameters, $F_s$, $i_1$, $i_2$, $G_{m1}$, $C_1$, $C_2$, the equivalent discrete-time $\Delta \Sigma$ modulator feedback coefficients, $a_1$ and $a_2$, are evaluated as

$$a_1 = \frac{G_{m1}i_1}{C_1C_2F_s^2},$$

(2.8)

and

$$a_2 = \frac{a_1}{2} + \frac{i_2}{C_2F_s}.$$  

(2.9)
From the above equations, it can be seen that if the reference-currents, $i_1$ and $i_2$, the transconductance of the amplifier, $G_{m1}$, and the clock frequency, $F_s$, all increase (or decrease) with the same proportionality constant, then the equivalent discrete-time $\Delta\Sigma$ modulator feedback coefficients, $a_1$ and $a_2$, and its discrete-time NTF do not change. Simultaneously scaling the reference-currents and the clock frequency does not change the performance, in terms of a resolution and a number of bits, of the continuous-time $\Delta\Sigma$ A/D converter. The fact that the ideal continuous-time $\Delta\Sigma$ A/D converters can be programmed with scalable reference-currents and clock frequencies, and always achieve the same resolution and the number of bits, can be used to achieve a wide-dynamic-range A/D conversion. It can be shown that the scaling of the reference-currents and the clock-frequency by an arbitrary constant, $K$, increases the dynamic range, or signal-to-quantization-noise (SQNR), of the A/D converter by $\log_2(K)$. If the programmable $\Delta\Sigma$ modulator has two states, state 1
and state 2, and in state 2, the reference-current, $S_2$, and the clock frequency, $F_{s2}$, are $K$ times larger than the corresponding values of $S_1$ and $F_{s1}$ in state 1, then the overall dynamic-range of the programmable A/D converter, $DR$, and the dynamic ranges of the A/D converter in each of the states, $DR_1$ and $DR_2$, are expressed as

$$DR = S_2 - N_1,$$  \hspace{1cm} (2.10)

$$DR_1 = S_1 - N_1,$$  \hspace{1cm} (2.11)

and

$$DR_2 = S_2 - N_2,$$  \hspace{1cm} (2.12)

where $N_1$ and $N_2$ are the in-band quantization-noise powers of the $\Delta \Sigma$ A/D converter in state 1 and state 2, respectively, and $S_1$ and $S_2$ are the reference-current-values in state 1 and state 2, respectively. Because in both states, state 1 and state 2, the continuous-time $\Delta \Sigma$ A/D converter achieves an identical performance, in terms of the dynamic ranges, $DR_1 = DR_2$, the in-band quantization-noise power in state 1, $N_1$, must be $K$ times lower than $N_2$ in state 2, and the dynamic range of the programmable A/D converter, $DR$, is given by

$$DR = DR_1 + 20 \log_{10}(K).$$ \hspace{1cm} (2.13)

Dynamic range of the A/D converter, $DR$ (dB), is related to its resolution, $B$ (bits), by $DR = 6.02B + 1.76$, and the system resolution, $B$, improvement over the resolutions in each state, $B_1 = B_2$, is expressed as

$$B = B_1 + \log_2(K).$$ \hspace{1cm} (2.14)
To verify the above conclusions, an Hspice simulation of the continuous-time ∆Σ A/D converter model with ideal components, and the following circuit parameters in state 2,

\[ C_1 = 10.52 \text{ pF}, \ C_2 = 3.97 \text{ pF}, \ i_1 = 880 \text{ nA}, \ i_2 = 707 \text{ nA}, \ G_m1 = 3.97 \mu\text{A}, \ F_{s1} = 1 \text{ MHz}, \]

is executed. With the scaling factor of \( K = 100 \), the overall dynamic-range of the programmable continuous-time ∆Σ A/D converter increases by 40 dB, and the resolutions increases by 6.6 bits, as shown in Fig. 2.12.

![2nd order CT Delta-Sigma / Behavioral Simulation](image)

Fig. 2.12. Programmable second-order continuous-time ∆Σ A/D converter behavioral simulation.

### 2.4.3 Anti-Aliasing and Input-Noise Integration

Continuous-time ∆Σ A/D converter can be represented with an equivalent model, where the sampling of a continuous-time signal takes place at the input of ∆Σ mod-
ulator, rather than at the quantizer, as shown in Fig. 2.13.

As derived in [34], the anti-aliasing pre-filter transfer-function for the continuous-time second-order $\Delta \Sigma$ A/D converter is expressed as

$$|STF(f)| = \left| \frac{1 - e^{-j2\pi f}}{2\pi f} \right|^2 = \left| \frac{\sin(\pi f)}{\pi f} \right|^2,$$

(2.15)

where $f$ is the continuous-time frequency of the input-signal. The continuous-time pre-filter behaves as an anti-aliasing filter, and is another reason for the popularity of the continuous-time $\Delta \Sigma$ A/D converter.

In the time domain, the impulse-response of the filter depends on the order of the $\Delta \Sigma$ modulator. For the continuous-time first-order $\Delta \Sigma$ A/D converter, the impulse-response of the anti-aliasing filter, $Sinc_1$, is a box with a duration equal to the $t_s$ sampling-period, for the second-order $\Delta \Sigma$ A/D converter, the impulse-response is $Sinc_2$, and for the third-order it is $Sinc_3$, as shown in Fig. 2.14. The frequency-responses of the $Sinc_1$, $Sinc_2$, and $Sinc_3$ filters are shown in Fig. 2.15, where $f_s$ is the sampling-frequency.

If the input to the continuous-time $\Delta \Sigma$ A/D converter is a white-noise corrupted DC-signal, i.e. photo-detector current with shot-noise, the anti-aliasing filters will
Fig. 2.14. Impulse-responses of $Sinc_1$, $Sinc_2$, and $Sinc_3$ anti-aliasing pre-filters.

Lowpass-filter the white-noise before the sampling. To determine the effectiveness of the anti-aliasing filters, $Sinc_1$ and $Sinc_2$, in filtering the input white-noise, noise-bandwidth (NBW) of those filters, $NBW_1$ and $NBW_2$, respectively, must be evaluated. Noise-bandwidth of a filter, $H(f)$, is defined as [34]

$$NBW = \frac{1}{2\pi} \int_{0}^{+\infty} \left| \frac{H(j\omega)}{H_{\text{max}}} \right|^2 d\omega.$$  \hspace{2cm} (2.16)

where $H_{\text{max}}$ is the maximum of the filter-transfer function. Using Parseval’s identity, one can estimate the noise-bandwidths $NBW_1$ and $NBW_2$ as

$$NBW_1 = \int_{0}^{t_s} 1^2 dt = t_s,$$  \hspace{2cm} (2.17)

and
Whereas noise power increases due to integration, the integrated signal power also increases proportional to $t_s^2$ for $Sinc_1$, and $t_s^4$ for $Sinc_2$. Therefore the signal-to-noise ratio (SNR) improves by passing through the input signal through the filter. SNR improves by 3-dB per octave for $Sinc_1$, and by 12-dB per octave for $Sinc_2$. Note, that in common imaging-sensors, the integration time is quite long, while the $t_s$ sampling time of the ∆Σ A/D converter is quite small. Therefore one might assume that using continuous-time ∆Σ A/D converter will not achieve such a high signal-to-noise ratio. But ∆Σ A/D converter output is filtered by a lowpass-filter. Assuming an ideal lowpass brick-filter at the output of the A/D converter, the output noise can be estimates as
\begin{equation}
O_{\text{noise}}_1 = \frac{t_s}{OSR},
\end{equation}

and

\begin{equation}
O_{\text{noise}}_2 = \frac{t_s^2}{OSR},
\end{equation}

where, $O_{\text{noise}}_1$ and $O_{\text{noise}}_2$ are the output noise of a first-order and second-order $\Delta \Sigma$ A/D converters respectively, given a unity white-noise inputs. Therefore the A/D converter improves the signal-to-noise ratio of the input signal as expressed in

\begin{equation}
SNR_1 = t_s OSR,
\end{equation}

and

\begin{equation}
SNR_2 = \frac{t_s^2 OSR}{2}.
\end{equation}

To verify the above conclusions, we analyzed the noise-performance of two filters, $Sinc_1$ and $Sinc_2$, in discrete-time, and different number of filter coefficients, or length. The four filters, simulated in Matlab, and their impulse-responses are:

Running-average filter (N=4),

\begin{equation}
y(n) = x(n) + x(n - 1) + x(n - 2) + x(n - 3),
\end{equation}

Repeating running-average filter (N=4),
\[ y(n) = x(n) + (x(n) + x(n-1)) \]
\[ + (x(n) + x(n-1) + x(n-2)) \]
\[ + (x(n) + x(n-1) + x(n-2) + x(n-3)) \]
\[ = 4x(n) + 3x(n-1) + 2x(n-2) + x(n-3), \]

and multi-path running-average filter \((N=7)\),

\[ y(n) = x(n) + 2x(n-1) + 3x(n-2) \]
\[ + 4x(n-3) + 3x(n-4) + \]
\[ 2x(n-5) + x(n-6), \]

where \(N\) is the number of filter coefficients, or length, \(x(n)\) is filter input, \(y(n)\) is filter output.

Impulse-response functions and frequency-transfer functions of the four filters are shown in Fig. 2.16 and Fig. 2.17, respectively.

Signal-to-noise-ratio at the output of all four filters, \(\text{Sinc}_1\), \(\text{Sinc}_2\), modified \(\text{Sinc}_2\), and long \(\text{Sinc}_1\), are simulated in Fig. 2.18. The most interesting outcome of this simulations is that a double integration, while generates a sharper filter, does not improve the signal-to-noise ratio at the output of the A/D converter any better than a simple long-integration.

Therefore while continuous time second order \(\Delta \Sigma\) and third order \(\Delta \Sigma\) A/D converters can achieve lower quantization noise, they do not necessarily improve on the input-noise (e.g. photo-detector shot noise). To suppress the input shot-noise of the photo-detector, a long single-integration might is the best option.
2.5 Summary

Various dynamic range enhancements methods for A/D converters are discussed in this chapter. Programmable-gain amplifiers are used mostly with voltage-input signals, to improve the sensor signals signal-to-noise ratio or to match the signal to the maximum A/D converter input-range, to improve the signal-to-quantization noise ratio at the output of the A/D converter. For current-input signals, a programmable current-integration is used to convert the input-current to a voltage-signal, that is matched to a fixed-resolution voltage-input A/D converter. All the above mentioned methods require a complex circuitry, i.e. a transimpedance amplifier or an instrumentation amplifier, and consume large power, i.e. high-resolution A/D converters always operates at maximum-speeds and maximum-power. The proposed ΔΣ A/D converter combines the programmability feature of the ΔΣ A/D converter with a
Fig. 2.17. Discrete-time Sinc filters - frequency-response simulations in Matlab.

current-integration of the continuous-time ΔΣ to achieve a wide-dynamic-range, because of programmable reference-currents, and low power, because of programmable clock-frequencies.
Fig. 2.18. Discrete-time Sinc filters - SNR simulations in Matlab.
3.1 Introduction

The circuit design of the programmable current-input second-order continuous-time ∆Σ A/D converter chip, operating at a nominal power supply voltage of $V_{DD} = 5 \, \text{V}$, is described in this chapter. The chip has been fabricated in MOSIS AMI 1.5 μm single-poly, double-metal, N-well CMOS process, and its layout is shown in Fig. 3.1. The system diagram of the components, built on this chip, are shown in Fig. 3.2. Reference-currents of the continuous-time ∆Σ A/D converter and the bias-current of the on-chip current-controlled oscillator are generated with a programmable current-reference D/A converter. A photodetector is integrated on-chip for light-measurement applications.

The building blocks, shown in Fig. 3.2, and their CMOS circuit designs are discussed in detail in this chapter.
3.2 Programmable A/D Converter

A programmable continuous-time second-order $\Delta \Sigma$ A/D converter is designed and fabricated using the MOSIS AMI 1.5 $\mu$m single-poly, double-metal, N-well, CMOS process. The supply-voltage, $V_{DD}$, for this process is specified as 5 V. A circuit model of a continuous-time second-order $\Delta \Sigma$ A/D converter is shown in Fig. 3.3, where $QZ$ is the A/D converter single-bit quantizer, and $Buffer$ is the input-current variable-bandwidth buffer. The reference-currents are noted as $i1$ and $i2$, the photodetector-current as $ipd$, the transconductance of the amplifier as $Gm1$, and the integrating capacitors as $C1$ and $C2$. 

Fig. 3.1. Programmable second-order continuous-time $\Delta \Sigma$ A/D converter layout.
3.2.1 Photo-Detector

The input to the A/D converter is multiplexed between an external current-source and the on-chip photo-detector. The photo-detector layout is shown in Fig. 3.4. The photo-detector is implemented with four diodes connected in parallel, where each of the diodes is implemented using a PN junction formed between the N-well and the P-substrate of the chip. Each N-well has an 8 µm by 8 µm area, the P+ diffusion has an 4 µm by 4 µm area and is separated from the N-well by 20 µm distance. The
photo-detector can easily deliver a 1 mA current under bright illumination obtained using a high-level microscope light.

![Photo-detector layout in 0.5 µm CMOS.](image)

**Fig. 3.4.** Photo-detector layout in 0.5 µm CMOS.

### 3.2.2 Input-Current Buffer

The input-current, whether from an external current-source or the on-chip photo-detector, is buffered with a variable-bandwidth current-buffer. The input-current buffer design was adopted from [26]. The input-current buffer schematic is shown in Fig. 3.5, where $i_{pd}$ is the photo-detector current, $v_{pd}$ is the photo-detector bias-voltage, and the $i_{out}$ is the buffer output-current. The layout of the current-buffer is shown in Appendix A.2.

The buffer allows for biasing the photo-detector with a fixed voltage, and presenting a low-impedance to the photo-detector’s current. Another benefit of this input-current buffer is its input-current-dependent bandwidth, and the input-current-dependent noise. To achieve higher resolution at lower input-current levels, the noise of the front-end buffer has to decrease, and if the noise is photo-detector-shot-noise.
dominated, then the lowering of the bandwidth of the buffer increases the signal-to-
noise-ratio of the buffer output-current. The Hspice simulations of the current-buffer
bandwidth versus variable input-current levels are shown in Fig. 3.6.

![Photo-detector self-biased buffer](image1)

**Fig. 3.5. Photo-detector self-biased buffer.**

![Input buffer bandwidth vs. input current](image2)

**Fig. 3.6. Input buffer bandwidth vs. input current.**
There are a few potential disadvantages to using this buffer. Its negative-feedback configuration is unstable at ultra-low input-current levels. The buffer’s instability at low input-current levels can be confirmed from the large loop-delays. Hspice simulations of the loop-delays at high- and low-current levels are shown in Fig. 3.7 and Fig. 3.8, respectively. To make the input-buffer stable at ultra-low current-levels, the photo-detector bias-voltage, $v_{pd}$, must be increased. Increasing the photo-detector bias-voltage at low current-levels, increases the photo-detector dark-current noise, and therefore degrades the performance of the current-buffer at low input-current levels.

![Fig. 3.7. Input-buffer step-response: high input-current.](image)

### 3.2.3 Current-Feedback D/A Converter

An important sub-circuit of the continuous-time $\Delta\Sigma$ A/D converter is the current-feedback single-bit D/A converter. The schematic of the current-feedback D/A converter is shown in Fig. 3.9, where $Qn$ and $Qp$ are the outputs of the A/D quantizer and $i1$ is the reference current. The layout in Appendix A.1. The feedback-
current D/A converters are implemented as cascaded current-mirrors to achieve a large output-resistance. The current-feedback D/A converter is controlled with $Q_n$ and $Q_p$ outputs of the A/D converter.

The current-feedback is not symmetric because there are two different mechanisms responsible for the turning of the feedback D/A converter, on and off. The rise and fall-times asymmetry in the feedback-current D/A converter Hspice simulations are shown in Fig. 3.10. The rise and fall times asymmetry, in the current-feedback D/A converter, increases the in-band white noise-floor in the output of the continuous-time $\Delta\Sigma$ A/D converter [1]. Hspice simulations of an ideal continuous-time $\Delta\Sigma$ A/D converter, with ideal circuit components, with and without feedback asymmetry are shown in Fig. 3.11.
Fig. 3.9. Current-feedback D/A converter schematic.

Fig. 3.10. Current-feedback D/A converter rise and fall times.
3.2.4 Operational Transconductance Amplifier

Continuous-time ∆Σ A/D converters require continuous-time integrators. There are three main categories of continuous-time integrators; MOSFET-C, Gm-C, and Gm-OTA-C [30]. The Gm-C design is the most suitable architecture due to its current-programmability feature, low-power and small area [30]. Tuning of Gm-C integrators can be accomplished by changing the capacitor sizes to achieve high linearity [8], or by changing the transconductance amplifier bias-currents, that is more suitable for out application.

The operational transconductance amplifier (OTA) is implemented as a two-stage differential amplifier [23]. The amplifier schematic is shown in Fig. 3.12, where $V_p$ and $V_m$ are the positive and negative inputs, respectively, and $I_{bias\text{-amp}}$ is the bias current of the amplifier. The amplifier layout is shown in Appendix A.3.
Because of the high supply voltage is 5 V in the MOSIS AMI 1.5 \( \mu \text{m} \) process, all current-mirrors of the amplifier are cascoded to increase the amplifier gain. The amplifier must operate in the sub-threshold bias range, where the gain is constant and the bandwidth increases with increasing bias currents, as shown in Fig. 3.13.

One significant problem associated with using Gm-C integrators in continuous-time \( \Delta \Sigma \) A/D converters, is the fact that the voltages on the integration-capacitors tend to oscillate near DC-voltages that increase proportionally with the input-current value. Therefore, the input-range of the transconductance amplifier, where the amplifier is linear becomes a limiting factor. The amplifier input-range is improved by using
degeneration diode-connected MOSFETs, connected in series with the differential-pair of the amplifier.

Fig. 3.13. Operational transconductance amplifier bandwidth vs. bias-current.

3.2.5 Continuous-Time Second-Order $\Delta \Sigma$ A/D Converter

In designing a current-input continuous-time $\Delta \Sigma$ A/D converter, there are several parameters available: the clock-frequency, the integration-capacitor values, the feedback-current values, and the amplifier transconductance values.

For a given clock frequency, high feedback-currents are needed. If the feedback-currents are low, the settling time of the feedback-current D/A converters is long and the feedback-delay will degrade the performance of the continuous-time $\Delta \Sigma$ A/D converter. Concurrently, the feedback-currents cannot be too high, otherwise they will cause large voltage-variations on the integration-capacitors, and the limited input-range and the slewing of the transconductance amplifier will degrade the performance of the continuous-time $\Delta \Sigma$ A/D converter. To decrease the voltage-variations on the
integration-capacitors, the capacitor values can be increased.

The transconductance amplifier must be biased with small bias-currents or designed with large transistors to operate in the sub-threshold bias range.

The two integration-capacitors of the continuous-time second-order $\Delta \Sigma$ A/D converter are implemented with poly-to-poly capacitors, available in the MOSIS AMI 1.5 $\mu$m process: $C_1 = 10.52$ pF (130 $\mu$m x 130 $\mu$m) and $C_2 = 3.97$ pF (80 $\mu$m by 80 $\mu$m).

Transistor-level simulations in Hspice of the second-order continuous-time $\Delta \Sigma$ A/D converter with different programmable settings of the reference currents and clock frequency are shown in Fig. 3.14. The following parameters are used: clock frequency $F_s = 1$ MHz, reference-currents $I_{ref1} = 4.4$ $\mu$A and $I_{ref2} = 3.5$ $\mu$A, amplifier transconductance $G_{m1} = 4$ $\mu$A/V, and amplifier bias-current $I_{amp} = 0.8$ $\mu$A.

The A/D converter power and energy-per-sample values are simulated in Hspice for different programmable settings are shown in Table 3.1. The energy-per-sample of the A/D converter is calculated based on oversampling ratio, or number of clock cycles per sample, $OSR = 1024$. Ideally, the energy-per-sample does not change with programmability, because the number of clock cycles required to achieve a single conversion is constant and equal to the oversampling ratio $OSR = 1024$.

The A/D converter latency-time, or time-per-sample, increases with smaller clock-frequencies, but the resolution must stay constant. Hspice simulations of $\Delta \Sigma$ A/D converter are not reliable in the absence of a small input-noise, especially with DC-inputs, therefore least-significant-bit (LSB) values are not consistent with ideal $\Delta \Sigma$
Fig. 3.14. Programmable second-order continuous-time ΔΣ A/D converter schematic simulation.

Table 3.1. Programmable continuous-time second-order ΔΣ A/D converter power Hspice simulations.

<table>
<thead>
<tr>
<th>$I_{VDD}$</th>
<th>$P_{VDD}$</th>
<th>Energy/sample</th>
</tr>
</thead>
<tbody>
<tr>
<td>19.2 μA</td>
<td>96.0 μW</td>
<td>98.3 nJ/sample</td>
</tr>
<tr>
<td>4.8 μA</td>
<td>24.0 μW</td>
<td>98.3 nJ/sample</td>
</tr>
<tr>
<td>1.2 μA</td>
<td>6.0 μW</td>
<td>98.3 nJ/sample</td>
</tr>
<tr>
<td>0.3 μA</td>
<td>1.5 μW</td>
<td>98.3 nJ/sample</td>
</tr>
</tbody>
</table>
models predictions. The A/D converter Hspice simulations of latency-time and resolution for different programmable settings are shown in Table 3.2.

Table 3.2. Programmable continuous-time second-order $\Delta\Sigma$ A/D converter latency-time and LSB Hspice simulations.

<table>
<thead>
<tr>
<th>$F_s$</th>
<th>$T_s$</th>
<th>Data Rate</th>
<th>Latency Time</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000.0 MHz</td>
<td>1.02 ms</td>
<td>980.0 Samples/s</td>
<td>1.02 ms</td>
<td>1.9 pA</td>
</tr>
<tr>
<td>250.0 kHz</td>
<td>4.2 ms</td>
<td>240.0 Samples/s</td>
<td>4.2 ms</td>
<td>3.8 pA</td>
</tr>
<tr>
<td>62.5 kHz</td>
<td>16.4 ms</td>
<td>61.0 Samples/s</td>
<td>16.4 ms</td>
<td>122.0 pA</td>
</tr>
<tr>
<td>15.6 kHz</td>
<td>65.8 ms</td>
<td>15.2 Samples/s</td>
<td>65.8 ms</td>
<td>1.9 pA</td>
</tr>
<tr>
<td>3.9 kHz</td>
<td>264.0 ms</td>
<td>3.8 Samples/s</td>
<td>264.0 ms</td>
<td>-.-</td>
</tr>
</tbody>
</table>

3.3 Reference-Current D/A Converter

The reference-currents of the continuous-time $\Delta\Sigma$ A/D converter, as well as the bias-current of current-controlled on-chip oscillator, are programmed with a current D/A converter. The current D/A converter schematic is shown in Fig. 3.15, where $[b_0, b_1, b_2, b_3, b_4]$ are the five control-bits, $I_{bias\_dac}$ is the D/A converter base-current, and $idac\_out$ is the output-current of the D/A converter. The current D/A converter has 5 stages, where each stage implements divide-by-4. Reference-current D/A converter layout is shown in Appendix A.4.

The programmable reference-current D/A converter power Hspice-simulations for different programmable settings are shown in Table 3.3. The supply voltage, $V_{DD}$, is equal to 5 V in power calculations. Because the D/A converter is a divider-type, it consumes a minimum of 37.8 $\mu$A standalone supply-current.

The programmable reference-current D/A converter linearity is not critical for the performance of the overall system, because if the reference-currents of the A/D
Fig. 3.15. Reference-current D/A converter schematic.

Table 3.3. Reference-current D/A converter power Hspice simulations.

<table>
<thead>
<tr>
<th>Bits</th>
<th>$I_{VDD}$</th>
<th>$P_{VDD}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10000</td>
<td>94 $\mu$A</td>
<td>470 $\mu$W</td>
</tr>
<tr>
<td>01000</td>
<td>52 $\mu$A</td>
<td>260 $\mu$W</td>
</tr>
<tr>
<td>00100</td>
<td>42 $\mu$A</td>
<td>208 $\mu$W</td>
</tr>
<tr>
<td>00010</td>
<td>39 $\mu$A</td>
<td>194 $\mu$W</td>
</tr>
<tr>
<td>00001</td>
<td>38 $\mu$A</td>
<td>190 $\mu$W</td>
</tr>
</tbody>
</table>

converter and the bias-current of the oscillator, all experience the same linearity-error, the overall equivalent discrete-time $\Delta \Sigma$ modulator parameters won’t change, and thus the A/D converter performance from the point of view of quantization noise is invariant under linearity-errors of the reference-current D/A converter.

3.4 Three-Stage Current-Controlled Ring-Oscillator

The programmable continuous-time second-order $\Delta \Sigma$ A/D converter requires programmable reference-currents as well as a programmable clock-frequency. A current-
controlled ring-oscillator can be seamlessly integrated into the global-scheme of programmable-current $\Delta \Sigma$ A/D converter [23]. A three-stage current-controlled ring-oscillator with three poly-to-poly inter-stage capacitances of 1 pF each is designed. The schematic of the oscillator is shown in Fig. 3.16, where $I_{bias\_osc}$ is the oscillator bias-current. The layout of the oscillator is shown in Appendix A.5.

![Fig. 3.16. Three-stage current-controlled ring-oscillator.](image)

The frequency, $F_{OSC}$, of the current-controlled ring-oscillator with $N$ number of stages, $V_{DD}$ supply-voltage, and $C_{TOT}$ inter-stage capacitance-values, is proportional to $I_{BIAS}$ and is expressed by [23]

$$F_{OSC} = \frac{I_{BIAS}}{NC_{TOT}V_{DD}},$$

(3.1)
where $I_{BIAS}$ is the bias-current of the oscillator.

The oscillator Hspice-simulation results, for the supply-voltage of $V_{DD} = 5$ V, are shown in Table 3.4. Reducing the oscillator frequency from 1.01 MHz to 4.3 kHz, i.e. by a factor of 234, reduces the oscillator current-consumption from 80.5 $\mu$A to 25.6 $\mu$A, i.e. by a factor of 3.14. In Hspice simulations, the oscillator is driving two 100 fF capacitors.

Table 3.4. Three-stage current-controlled ring-oscillator power Hspice simulations.

<table>
<thead>
<tr>
<th>$I_{bias_{-osc}}$</th>
<th>$F_s$</th>
<th>$T_s$</th>
<th>$I_{V_{DD}}$</th>
<th>$P_{V_{DD}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>19.2 $\mu$A</td>
<td>1010.0 kHz</td>
<td>1.0 $\mu$s</td>
<td>80.5 $\mu$A</td>
<td>402 $\mu$W</td>
</tr>
<tr>
<td>4.9 $\mu$A</td>
<td>233.0 kHz</td>
<td>4.3 $\mu$s</td>
<td>41.0 $\mu$A</td>
<td>205 $\mu$W</td>
</tr>
<tr>
<td>1.3 $\mu$A</td>
<td>59.5 kHz</td>
<td>17.0 $\mu$s</td>
<td>29.4 $\mu$A</td>
<td>147 $\mu$W</td>
</tr>
<tr>
<td>0.333 $\mu$A</td>
<td>15.0 kHz</td>
<td>66.7 $\mu$s</td>
<td>26.7 $\mu$A</td>
<td>133 $\mu$W</td>
</tr>
<tr>
<td>0.095 $\mu$A</td>
<td>4.3 kHz</td>
<td>234.0 $\mu$s</td>
<td>25.6 $\mu$A</td>
<td>128 $\mu$W</td>
</tr>
</tbody>
</table>

3.5 Summary

A programmable second-order continuous-time $\Delta\Sigma$ A/D converter was designed and fabricated using MOSIS AMIS 0.5 $\mu$m CMOS process. A continuous-time $\Delta\Sigma$ A/D converter was designed to achieve a 12-bit dynamic-range with an oversampling ratio of 1024. By using programmable reference-currents and programmable clock-frequency, the dynamic-range of the $\Delta\Sigma$ A/D converter increases to an equivalent of 20-bits. The 8-bit dynamic-range improvement is the result of decreasing the reference-currents and the clock-frequency of the A/D converter by a factor of 256 with a programmable current D/A converter.

By reducing the reference-currents and simultaneously, reducing the clock-frequency the power consumption of the $\Delta\Sigma$ A/D converter, the on-chip current-controlled os-
cillator, and the reference-current D/A converters decreases. Reducing the reference-currents from 4.4 $\mu$A to 17.2 $n$A, i.e. by a factor of 256, decreases the A/D converter supply-current from 19.2 $\mu$A to 0.3 $\mu$A, i.e. by a factor of 64. And the reduction of the clock-frequency from 1 MHz to 4 kHz decreases the current-controlled oscillator supply-current from 80.5 $\mu$A to 25.6 $\mu$A, i.e. by a factor of 3.1.

Because, during programming of the $\Delta\Sigma$ A/D converter clock-frequency, the oversampling ratio, or the number of clock-cycles per sample, does not change, the overall A/D conversion time decreases proportional to the clock-frequency. Thus, programmability lowers the power consumption of the system, but increases the energy-per-sample. The increased energy-per-sample, at lower clock-frequencies and lower reference-currents, is expected to be lower than that of the equivalent non-programmable high-resolution A/D converter.
4.1 Introduction

The circuit design of a programmable current-input third-order continuous-time ΔΣ A/D converter, with an on-chip RF-power rectifier, voltage regulator, and voltage and current-reference circuits, operating at a nominal supply-voltage of $V_{DD} = 3$ V, is described in this chapter. The chip was fabricated using MOSIS ON 0.5 µm double-poly, triple-metal, N-well, CMOS process. The chip layout is shown in Fig. 4.1, and the system diagram of the components built on this chip is shown in Fig. 4.2.

The design of individual-components on this chip is discussed in this chapter. The on-chip programmable A/D converter is a third-order continuous-time ΔΣ A/D converter with its reference-currents being programmed with a current-reference D/A converter. The RF-power rectifier and the voltage regulator are designed to generate a stable 3 V supply-voltage. All the necessary reference-voltages, and reference-currents of the A/D converter are generated on-chip. The A/D converter clock-signal
is generated with an on-chip current-controlled oscillator, that derives its power, as the rest of the circuits, from a DC-rectified RF-power.

Fig. 4.2. RF-powered programmable A/D converter system diagram.
A few major modifications are included in this new design, compared to the design presented in Chapter 3:

1. The order of the ∆Σ A/D converter is increased from two to three, to achieve a 12-bit resolution with an oversampling ratio, or a number of clock cycles-per-sample, OSR = 128, compared to an OSR = 1024 for the second-order ∆Σ.

2. All on-chip circuits, including the on-chip current-controlled oscillator, are optimized to achieve a low-power operation. The supply-current of the chip, by design, is less than 40 µA, and the supply voltage is, nominally, equal to 3 V. In comparison, the previously-designed programmable continuous-time second-order ∆Σ A/D converter consumed more than 200 µA of supply-current, including the current of the on-chip oscillator, with the supply voltage equal to 5 V.

3. The third-order continuous-time ∆Σ A/D converter now has a novel feedback / feed-forward architecture, that yields a more robust design against the process variations, and the circuit non-linearities [37].

4. Current feedback-circuits of the continuous-time ∆Σ A/D converter are redesigned to achieve a symmetric feedback pulses, with equal rise and fall-times, to lower the feedback error that appears as a white-noise source at the input.

5. The input-current buffer, believed to be responsible for the instabilities at ultra-low input-current levels, is not used. Because the voltage variations on the first integrating capacitor, in this new design of the continuous-time ∆Σ A/D converter, are constrained to less than 100 mV, the directly-connected photo-detector output-current will not be significantly affected.
6. Supply voltage is reduced from 5 V to 3 V, to lower the power consumption. As a result, all current-mirrors were re-designed as low-voltage cascode mirrors [23].

7. All the voltage and current-references are generated on-chip with bandgap voltage-reference and beta-multiplier current-reference circuits [23].

4.2 RF-Power Rectifier, Voltage-Limiter and Voltage-Regulator

An RF-power rectifier is required to convert the incoming RF-power to an unregulated DC-voltage. The power conversion must have high-efficiency to achieve a long-range operation of a wireless sensor, because the available, to the sensor, RF-power decreases with the square of the distance between the reader and the sensor chip. The RF-power to DC-voltage conversion chain most commonly consists of an RF-power rectifier, a voltage limiter, a storage capacitor, and a voltage regulator [7, 24].

4.2.1 RF-Power Rectifier

The circuit design of the RF-power rectifier is based on the Cockcroft-Walton multiplying circuit with schottky diodes [25]. The RF-power rectifier is designed with nine stages, to generate a 3 V DC-voltage with a 2 mW available-power 350 MHz frequency RF-source, and a 1 $\mu$A load-current. Each stage of the RF-power rectifier consists of an inter-stage poly-to-poly capacitor, with an area of 100 $\mu$m by 85 $\mu$m and the capacitance value of $C_i = 7.5$ pF, and a single-size schottky diode, available in MOSIS ON 0.5 $\mu$m CMOS process. The rectified DC-voltage is held onto a load-capacitance, with an area of 300 $\mu$m by 300 $\mu$m and the capacitance value of $C_L = 80$ pF. The RF-power rectifier schematic is shown in Fig. 4.3, and the layout in the Appendix B.1.
Without a voltage-regulator following the RF-power rectifier, the generated DC-voltage increases with an increase in the available RF-power, as shown with Hspice simulation in Fig. 4.4. To regulate the output DC-voltage of the RF-power rectifier to a nominal supply voltage of $V_{DD} = 3$ V, independent of the incoming RF-power, a voltage-regulator and a voltage-limiter circuits must follow the RF-power rectifier circuit.

4.2.2 Voltage-Limiter

The RF-power rectifier is followed by a voltage-limiter that protects the on-chip circuits from sudden surges in the incoming RF-power, and sudden surges in the on-chip rectified DC-voltage [6]. The circuit schematic of the voltage limiter is shown in Fig. 4.5, and the layout in Appendix B.2. Voltage limiter is a negative-feedback system, whose control line consists of nine diode-connected NMOS transistors, that
will turn on and shunt the 'excess' charge to ground when the limiter input-voltage, $V_{DD_{RF}}$, increases beyond 10 V. In Hspice simulations, the input to the voltage-limiter is a current, and the output is a limiter-voltage. When the input-current is swept from 100 pA to 10 mA, the output voltage of the voltage-limiter is stabilized around DC-voltage 10-V, after the input-current reaches 10 nA, as shown in Fig. 4.6.

4.2.3 Linear, Shunt Voltage-Regulator

The function of the voltage-limiter was to protect the on-chip circuits if the RF-power rectifier generates DC-voltages in excess of 10 V. The function of the shunt voltage-regulator, is to regulate the RF-power rectifier output DC-voltage to a nominal $V_{dd_{reg}} = 3$ V. The input of the voltage regulator is the output of the voltage limiter, $V_{dd_{LIM}}$. Linear, shunt voltage-regulator is designed as a two-stage amplifier in a negative resistive-feedback loop [19, 6]. The amplifier compensation capacitor is
a poly-to-poly capacitor with $C_c = 8.8$ pF value, and 100 $\mu$m by 100 $\mu$m area, and the feedback resistors are silicide-blocked poly-resistors with $R_1 = 550$ kOhm and $R_2 = 392$ kOhm values. The shunt voltage-regulator schematic is shown in Fig. 4.7, where $V_{dd\_reg}$ is the voltage-regulator output-voltage, and the $V_{dd\_lim}$ is the RF-power-rectified voltage-limiter output-voltage. The layout is shown in Appendix B.3.
Fig. 4.6. Voltage-limiter output-voltage vs input-current Hspice simulation.

Fig. 4.7. Linear, shunt voltage-regulator schematic.
The voltage regulator is a negative-feedback circuit whose stability is critical for the overall system performance under varying input RF-power conditions. Stability of the negative-feedback system can be characterized by analyzing its loop frequency-response and its loop phase-margin [20] or by analyzing its step-response. When the input to the voltage regulator is generated by a constant current-source of 1 mA charging a capacitor of 100 nF, the output-voltage of the voltage-regulator stabilizes to a nominal $V_{DD_{REG}} = 3\ \text{V}$ after only 2.5 ms, without much ringing. Hspice simulation results are shown in Fig. 4.8. Note, that the input and the output of the voltage regulator are directly connected, and the $C = 100\ \text{nF}$ capacitor at the input of the voltage-regulator, in Hspice simulations, can be considered to be the voltage-regulator load.

Fig. 4.8. Shunt voltage-regulator start-up transient-response Hspice simulation for a fixed input-current.

In power-limited applications, all on-chip circuits must be low-power, including the voltage-regulator. The voltage regulator circuit, together with the bandgap voltage-
reference circuit, current-reference circuit, and the on-chip current-input D/A converter circuit consume approximately 15 µA of supply current, or 45 µW power with a supply voltage of 3 V.

4.3 Bandgap Voltage-Reference and Beta-Multiplier Current-Reference

Because the programmable continuous-time ∆Σ A/D converter must be powered with an RF-source, all the reference-voltages and reference-currents, for the A/D converter operation, must be generated on-chip. These reference voltages and reference currents must be temperature, process, and supply voltage, (PTV), independent for the following two reasons.

1. The on-chip generated reference voltage is approximately equal to 1.2 V. Its most critical application is in the voltage-regulator, where it, directly, determines the voltage-regulator output-voltage, and therefore the supply-voltage, \( V_{DD} \), for every on-chip circuit. The supply-voltage variation will significantly affect the on-chip oscillator frequency, and therefore the continuous-time ∆Σ A/D converter performance, that depends on it.

2. The on-chip generated reference current is approximately equal to 200 nA. Its value is multiplied, with low-voltage current mirrors, and applied as the bias-current for the on-chip current-controlled ring-oscillator, and as reference currents for continuous-time third-order ∆Σ A/D converter. ∆Σ A/D converter can become unstable if its reference-currents and clock-frequency deviate significantly from the modeled values.

The design of only temperature and supply-voltage independent current- and voltage-reference circuits is pursued in this work, due to unavailability of the inter-die process-variation parameters for MOSIS ON 0.5 µm process.
4.3.1 Bandgap Voltage-Reference

Bandgap voltage-reference circuit schematic is shown in Fig. 4.9 and the layout in Appendix B.4. To generate a temperature-independent reference-voltage, a complementary-to-absolute-temperature (CTAT) voltage is added to a proportional-to-absolute-temperature (PTAT) voltage [23]. Forward-bias voltage of a diode, or a diode-connected bipolar-junction-transistor (BJT), is a CTAT voltage, assuming the current through the diode is constant with temperature. Bias-voltage difference, $V_{BE1} - V_{BE2}$, of two different-size forward-biased diodes, or diode-connected bipolar-junction-transistors (BJT), biased with identical currents, $I_{diode}$, is a PTAT voltage, expressed as [23]

$$V_{BE1} - V_{BE2} = V_T \ln(n), \quad (4.1)$$

where $n$ is the ratio of the diode, or BJT emitter, areas, and $V_T$ is the thermal voltage. The reference-voltage is expressed as

$$V_{ref} = I_{diode} R_1 + V_{diode}, \quad (4.2)$$

where $R_1$ is the resistance in the output, $I_{diode}$ is a supply-independent current, and $V_{diode}$ is a current-dependent diode forward-bias voltage. Because the diode forward-bias voltage, $V_{diode}$, and the diode current, $I_{diode}$, do not depend on the supply-voltage, $V_{DD}$, then the reference-voltage, $V_{ref}$, is supply-independent.

4.3.2 Beta-Multiplier Current-Reference

The beta-multiplier current-reference circuit schematic is shown in Fig. 4.10 and the layout in Appendix B.5.

The bandgap voltage-reference, the beta-multiplier current-reference, and the programmable current D/A converter circuits are simulated in Hspice, to analyze their
Fig. 4.9. Bandgap voltage-reference circuit schematic.

Fig. 4.10. Beta-multiplier current-reference circuit schematic.
performance with variable temperature, $T$, shown in Fig. 4.11, and with variable supply-voltage, $V_{DD}$, shown in Fig. 4.12. The reference-current circuit generates a nominal $I_{ref} = 200$ nA current, and the reference-voltage circuit generates a nominal $V_{ref} = 1.277$ V voltage.

![Graph showing reference-voltage and reference-current variations with temperature.](image)

**Fig. 4.11.** Reference-voltage and reference-current variations with the temperature, $T$, Hspice simulations.

The total current-consumption of the reference-generators and the programmable current D/A converter increases from 5.3 $\mu$A to 6.3 $\mu$A, when the temperature, $T$, increases from 10°C to 60°C and from 5.3 $\mu$A to 6.1 $\mu$A, when the supply voltage, $V_{DD}$ increases from 2.7 V to 3.3 V.

### 4.4 Programmable Continuous-Time Third-Order Feedback/Feed-Forward $\Delta \Sigma$ A/D Converter

A low-power programmable continuous-time third-order $\Delta \Sigma$ A/D converter is designed to achieve a 12-bit resolution with an oversampling ratio of OSR = 128. A
small oversampling ratio, or a small number of clock cycles-per-sample, of the A/D converter results in low energy-per-sample, and is important in RF-powered and battery-assisted applications.

Input of the continuous-time ∆Σ A/D converter is multiplexed between an external current-source and an on-chip photo-detector.

4.4.1 Photo-Detector

The photo-detector layout is shown in Fig. 4.13. The photo-detector consists of four PN-junction diodes connected in series, where each N+ diffusion-region has a 4 μm by 4 μm area, the N-well has 12 μm by 12 μm area, and the N-wells are separated from the closest P+ diffusion-regions by a 20 μm distance. The P+ diffusion-regions are 4 μm wide.
The photo-detector current is not buffered in this design. The photo-detector current is only mirrored with a low-voltage current-mirrors onto the first capacitor, as shown in Fig. 4.14, $I_{ref\_1\_a}$ and $I_{ref\_1\_b}$ are the low-voltage mirror bias currents.

Fig. 4.14. Input-current mirror in the continuous-time third-order $\Delta\Sigma$ A/D converter.
4.4.2 Current-Feedback D/A Converter

The current-feedback circuit of the continuous-time ∆Σ A/D converter is designed with a symmetry in mind. The feedback-circuit schematic is shown in Fig. 4.15, where $Q_p$ is the A/D converter one-bit output. The reference currents, $I_{ref1_a}$ and $I_{ref1_b}$, are mirrored with low-voltage current-mirrors.

![Schematic of Current-Feedback D/A Converter](image)

Fig. 4.15. Current-feedback in the continuous-time third-order ∆Σ A/D converter.

4.4.3 Operational Transconductance Amplifier

Continuous-time ∆Σ A/D converters require continuous-time integrators. Continuous-time integrators can be implemented as RC or Gm-C integrators [29]. Gm-C integrators were chosen for this design for their current-programmability feature. The operational transconductance amplifiers of the continuous-time Gm-C-integrators are designed as two-stage amplifiers. The schematic of the transconductance-amplifier is shown in Fig. 4.16, and the layout in Appendix B.8. Current-mirrors of the amplifier are based on low-voltage current-mirror architectures.
4.4.4 Continuous-Time Third-Order $\Delta\Sigma$ A/D Converter

The third-order continuous-time $\Delta\Sigma$ A/D converter parameters are calculated from a discrete-time $\Delta\Sigma$ model, using impulse invariant transformation to find the equivalent continuous-time $\Delta\Sigma$ modulator parameters. The model of the continuous-time $\Delta\Sigma$ A/D converter is shown in Fig. 4.17 and its discrete-time $\Delta\Sigma$ model in Fig. 4.18.

![Continuous-time CIFB/CIFF third-order $\Delta\Sigma$ A/D converter schematic model.](image)

Fig. 4.17. Continuous-time CIFB/CIFF third-order $\Delta\Sigma$ A/D converter schematic model.
Discrete-time $\Delta\Sigma$ model feedback coefficients, $a_1$, $a_2$, and $a_3$, are calculated so that the noise-transfer-function of the discrete-time $\Delta\Sigma$ modulator is a 3rd-order high-pass Chebyshev II filter with a corner frequency is equal to $W_n = \pi/128$, and the filter attenuation in the stopband is equal to $R = 80$ dB. The high-pass noise-transfer-function (NTF) and the feedback-coefficients are estimated to be

$$NTF(z) = \frac{z^3 - 3z^2 + 3z - 1}{z^3 - 2.343z^2 + 1.885z - 0.5156},\quad (4.3)$$

and

$$a_1 = 0.0265, \quad a_2 = 0.1991, \quad a_3 = 0.6569, \quad (4.4)$$

respectively. The pole-zero and the transfer-function of the NTF are plotted in Fig. 4.19 and Fig. 4.20. The pole-zero plot allows us to estimate how close the poles of the $\Delta\Sigma$ NTF are to its zeros. If the poles of the NTF are too close to the zeros, then the zeros will not be very effective in the quantization-noise suppression. The transfer-function of the NTF, on the other hand, allows us to estimate the stability of the $\Delta\Sigma$ modulator. If the value of the NTF at high frequencies is higher than 1.2 then modulator is a candidate for instabilities when the input-current becomes close to the reference-currents, according to the Lee’s principle [34].
To estimate the continuous-time third-order ∆Σ A/D converter parameters, i.e. the reference-currents, $i_1$, $i_2$, and $i_3$, the integration-capacitances, $C_1$, $C_2$, and $C_3$, the amplifiers’ transconductances, $G_{m1}$ and $G_{m2}$, and the clock frequency, $F_s$, we must rely on impulse-invariant transformations of discrete-time ∆Σ modulator parameters, i.e. the feedback coefficients, $a_1$, $a_2$, and $a_3$. The impulse-invariant transformation results can be expressed with either one of the following two sets of equations:

\[
G_{m1} = F_s C_1, \quad (4.5)
\]
\[
G_{m2} = F_s C_2, \quad (4.6)
\]
\[
i_1 = F_s C_1 a_1, \quad (4.7)
\]
\[
i_2 = F_s C_2 (a_2 - a_1), \quad (4.8)
\]
Fig. 4.20. Third-order Chebyshev 2 high-pass filter frequency response.

and

\[ i_3 = F_s C_3 (a_3 - \frac{a_2}{2} + \frac{a_1}{3}) \]  \hspace{1cm} (4.9)

or

\[ i_1 = F_s^3 \frac{C_1 C_2 C_3}{G_{m1} G_{m2}} a_1 \]  \hspace{1cm} (4.10)

\[ i_2 = F_s^2 \frac{C_2 C_3}{G_{m2}} (a_2 - a_1) \]  \hspace{1cm} (4.11)

and

\[ i_3 = F_s C_3 (a_3 - \frac{a_2}{2} + \frac{a_1}{3}) \]  \hspace{1cm} (4.13)

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Unlike the first design, described in Chapter 3, all reference-currents of the continuous-time ∆Σ A/D converter are generated on-chip, with a beta-multiplier current-reference circuit. Therefore, the choice of the continuous-time ∆Σ A/D converter parameters must not only satisfy the impulse-invariant equations, but also the physical-circuit implementation-constraints. For the circuit-implementation of the continuous-time third-order ∆Σ A/D converter, the following constraints were applied. All reference currents, $i_1$, $i_2$, and $i_3$, are equal to 1 µA, where we assumed that 1 µA is the maximum sensor-current of interest. The maximum clock-frequency is set equal to 1 MHz, as a result of trade-off between the low-power of the oscillator and the data-conversion speed of the A/D converter.

Knowing the continuous-time ∆Σ parameters, one can estimate the equivalent discrete-time ∆Σ modulator parameters as follows,

$$a_1 = \frac{i_1}{F_s C_1},$$

$$a_2 = \frac{i_2}{F_s C_2} + a_1,$$  \hspace{1cm} (4.14)

$$a_3 = \frac{i_3}{F_s C_3} + \frac{a_2}{2} - \frac{a_1}{3},$$  \hspace{1cm} (4.15)

and

$$a_3 = \frac{i_3}{F_s C_3} + \frac{a_2}{2} - \frac{a_1}{3},$$

$$NTF(z) = \frac{z^3 - 3z^2 + 3z - 1}{z^3 - 2.64z^2 + 2.43z - 0.764},$$  \hspace{1cm} (4.18)
and


d_1 = 0.026, \ a_2 = 0.15, \ a_3 = 0.36.

(4.19)

The schematic-derived pole-zero and NTF are shown in Fig. 4.21 and Fig. 4.22. The plots indicate a significant shift from the model, that require schematic transistor-level Hspice simulations of the \( \Delta \Sigma \) A/D converter to verify its performance.

![Third-Order Schematic NTF Model Pole-Zero](image)

Fig. 4.21. Discrete-time model pole-zero derived from schematic Hspice simulation.

The schematic transistor-level Hspice-simulation results for four programmable reference-currents and clock-frequencies are shown in Fig. 4.23. For decreasing reference-currents, decreasing input-currents were chosen in Hspice simulations, i.e. 637 nA (-5dB), 87 nA (-10.5dB), 23 nA (-9.8dB), 5.7 nA (-10dB).
Fig. 4.22. Discrete-time model NTF derived from schematic Hspice simulation.

The programmable $\Delta \Sigma$ A/D converter latency-time, or time-per-sample, and the least-significant-bit (LSB) of the A/D converter, estimated from the schematic Hspice simulations, are shown in Table 4.1. Decreasing the reference-frequency and the reference-currents, increases the conversion time of the A/D converter, but decreases the least-significant-bit (LSB), therefore increasing the dynamic-range of the A/D converter.

Table 4.1. Programmable third-order $\Delta \Sigma$ A/D converter latency-time and LSB Hspice simulations.

<table>
<thead>
<tr>
<th>$F_s$</th>
<th>Data Rate</th>
<th>Latency Time</th>
<th>LSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>1440.0 kHz</td>
<td>11.25 kSamples/s</td>
<td>0.089 ms</td>
<td>244.0 pA</td>
</tr>
<tr>
<td>335.0 kHz</td>
<td>2.6 kSamples/s</td>
<td>0.384 ms</td>
<td>6.1 pA</td>
</tr>
<tr>
<td>78.0 kHz</td>
<td>0.6 kSamples/s</td>
<td>1.65 ms</td>
<td>1.52 pA</td>
</tr>
<tr>
<td>19.0 kHz</td>
<td>0.148 kSamples/s</td>
<td>6.7 ms</td>
<td>0.38 pA</td>
</tr>
</tbody>
</table>
Fig. 4.23. Third-order continuous-time \(\Delta\Sigma\) A/D converter schematic Hspice simulation results.

Continuous-time \(\Delta\Sigma\) A/D converter power decreases with decreasing the reference-currents and the clock-frequency. Hspice-simulation results are shown in Table 4.2. In Hspice simulations, the A/D converter supply-voltage, \(V_{DD}\), is 3 V, and the output of the A/D converter drives two 100 fF capacitors.

Table 4.2. Third-order continuous-time \(\Delta\Sigma\) A/D converter power Hspice simulations.

<table>
<thead>
<tr>
<th>(I_{bias_adc})</th>
<th>(F_s)</th>
<th>(T_s)</th>
<th>(I_{VDD})</th>
<th>(P_{VDD})</th>
</tr>
</thead>
<tbody>
<tr>
<td>227.0 nA</td>
<td>1440.0 MHz</td>
<td>0.695 (\mu s)</td>
<td>7.6 (\mu A)</td>
<td>22.8 (\mu W)</td>
</tr>
<tr>
<td>58.5  nA</td>
<td>335.0 kHz</td>
<td>3.0 (\mu s)</td>
<td>2.3 (\mu A)</td>
<td>6.9 (\mu W)</td>
</tr>
<tr>
<td>14.3  nA</td>
<td>78.0 kHz</td>
<td>12.9 (\mu s)</td>
<td>1.4 (\mu A)</td>
<td>4.2 (\mu W)</td>
</tr>
<tr>
<td>3.6   nA</td>
<td>19.0 kHz</td>
<td>52.5 (\mu s)</td>
<td>1.2 (\mu A)</td>
<td>3.6 (\mu W)</td>
</tr>
</tbody>
</table>
4.5 Programmable Reference-Current D/A Converter

A programmable reference-current D/A converter is designed to achieve division ratios of 1, 4, 16, and 64. The D/A converter is controlled by four bits, b0, b1, b2, and b3. The schematic of the programmable D/A converter is shown in Fig. 4.24, where $I_{bias\_dac}$ is the D/A converter base-current, and $I_{0\_dac}$ is the output offset-current. The layout is shown in Appendix B.6. The output-currents of the programmable D/A converter, $I_{dac\_out}$, simulated with Hspice for the input-current $I_{bias\_dac} = 200$ nA, and multiple programmable-bits are shown in Table 4.3. The implemented current-division ratios of the D/A converter, 1, 3.88, 4.1, and 3.97, are close to the designed value of 4.

<table>
<thead>
<tr>
<th>Bits</th>
<th>$I_{dac_out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10000</td>
<td>94 nA</td>
</tr>
<tr>
<td>01000</td>
<td>52 nA</td>
</tr>
<tr>
<td>00100</td>
<td>42 nA</td>
</tr>
<tr>
<td>00010</td>
<td>39 nA</td>
</tr>
</tbody>
</table>

The D/A converter consumes a small, 300 nA, supply-current, that does not change significantly for different of input-bit combinations.

4.6 Five-Stage Current-Controlled Ring-Oscillator

To generate the clock-signal for the ΔΣ A/D converter, an on-chip oscillator is designed. A current-controlled ring-oscillator was chosen for its low-power, and programmable-current features. The schematic of the five-stage current-controlled ring-oscillator is shown in Fig. 4.25, where $I_{bias\_osc\_a}$ and $I_{bias\_osc\_b}$ are the oscillator bias-currents. The layout of the oscillator is shown in Appendix B.7. Because
the supply voltage, $V_{DD}$, is only 3 V, it is not possible to use cascode current-mirrors. Low-voltage current mirrors are used to lower the phase-noise of the oscillator. Number of stages of the oscillator is optimized to decrease the oscillator-power. The oscillator phase-noise decreases with decreasing oscillation-frequency. Therefore, at low bias-currents and low-frequencies of the oscillator, the oscillator phase-noise decreases, which improves the continuous-time ΔΣ A/D converter performance.

Hspice simulations of the five-stage current-controlled ring-oscillator are shown in Table 4.4, where $F_s$ is the oscillator frequency. The power consumptions of the oscillator decreases with lower frequencies, but the total energy over a fixed number of periods, i.e. oversampling ratio, OSR = 128, is increasing, i.e. 3.74 nJ, 6.33 nJ, 15.7 nJ, and 54.4 nJ.
Table 4.4. Five-stage current-controlled ring oscillator Hspice simulation results.

<table>
<thead>
<tr>
<th>( I_{bias_{osc}} )</th>
<th>( F_s )</th>
<th>( T_s )</th>
<th>( I_{VDD} )</th>
<th>( P_{VDD} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>1130.0 nA</td>
<td>1440.0 kHz</td>
<td>0.695 ( \mu s )</td>
<td>14.0 ( \mu A )</td>
<td>42.0 ( \mu W )</td>
</tr>
<tr>
<td>287.0 nA</td>
<td>335.0 kHz</td>
<td>3.0 ( \mu s )</td>
<td>5.5 ( \mu A )</td>
<td>16.5 ( \mu W )</td>
</tr>
<tr>
<td>70.2 nA</td>
<td>78.0 kHz</td>
<td>12.9 ( \mu s )</td>
<td>3.2 ( \mu A )</td>
<td>9.5 ( \mu W )</td>
</tr>
<tr>
<td>17.9 nA</td>
<td>19.0 kHz</td>
<td>52.5 ( \mu s )</td>
<td>2.7 ( \mu A )</td>
<td>8.1 ( \mu W )</td>
</tr>
</tbody>
</table>

The oscillator frequency changes slightly with temperature. The oscillator Hspice-simulation results for the bias-current of \( I_{bias_{osc}} = 1.13 \, \mu A \) and increasing temperature, from 10°C to 60°C, are shown in Table 4.5.

4.7 Summary

An RF-powered and programmable third-order continuous-time \( \Delta \Sigma \) A/D converter was designed and fabricated using MOSIS ON 0.5 \( \mu m \) CMOS process. The
Table 4.5. Five-stage current-controlled ring-oscillator Hspice simulation - frequency vs temperature.

<table>
<thead>
<tr>
<th>T (°C)</th>
<th>$F_s$ (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>1.48</td>
</tr>
<tr>
<td>20</td>
<td>1.456</td>
</tr>
<tr>
<td>30</td>
<td>1.432</td>
</tr>
<tr>
<td>40</td>
<td>1.409</td>
</tr>
<tr>
<td>50</td>
<td>1.387</td>
</tr>
<tr>
<td>60</td>
<td>1.366</td>
</tr>
</tbody>
</table>

RF-powered A/D converter includes an RF-power rectifier, a voltage regulator, a bandgap voltage and current-reference circuits, a third-order continuous-time $\Delta \Sigma$ A/D converter, a current-controlled five-stage ring-oscillator, and a programmable reference-current D/A converter circuit.

The RF-power rectifier generates a 3 V, nominal, DC supply voltage using a directly-connected, 2 mW RF-power source with 350 MHz frequency, and a 1 $\mu$A load-current. A voltage-limiter is included to protect the circuits from sudden increases in the DC supply-voltage above 10V. The on-chip voltage regulator, bandgap voltage and current-reference circuits are designed to provide a stable, nominal supply voltage of $V_{\text{DD}} = 3$ V, a reference-voltage of $V_{\text{ref}} = 1.25$ V, and a reference-current of $I_{\text{ref}} = 200$ nA. The voltage-regulator circuit consumes 15 $\mu$A current, whereas the voltage and current-references circuits, together with the on-chip programmable current D/A converter circuit, consume 5.5 $\mu$A current.

The continuous-time third-order $\Delta \sigma$ A/D converter was designed to achieve a 12-bit resolution, with an oversampling ratio of 128, and achieve a programmable dynamic-range of 18-bits. The 6-bit equivalent dynamic-range improvement in the A/D conversion is the result of decreasing the A/D converter reference-currents from 1 $\mu$A to 15.6 nA, i.e. a factor of 64. The third-order continuous-time $\Delta \Sigma$ A/D con-
verter achieves a dynamic-range that is comparable to the second-order $\Delta \Sigma$ performance, designed in Chapter 3, with a significantly less oversampling ratio, i.e. 128 compared to 1024.

To operate from an RF-power source, the continuous-time third-order $\Delta \Sigma$ A/D converter, and the five-stage current-controlled ring oscillator are designed as low-power and low-voltage circuits. Simultaneously decreasing the reference-currents, and the clock frequency, additionally decreases the power-consumption in the A/D converter and the oscillator, while increasing the dynamic-range of the A/D conversion. Decreasing the reference currents from 1.13 $\mu$A to 17.9 nA, i.e. a ratio of 63, decreases the A/D converter supply current from 7.6 $\mu$A to 1.2 $\mu$A, i.e. a ratio of 6.3. And simultaneously decreasing the on-chip current-controlled oscillator frequency from 1.44 MHz to 19 kHz, i.e. a ratio of 76, decreases the oscillator supply current from 14 $\mu$A to 2.7 $\mu$A, i.e. a ratio of 5.2.

As in the case of the programmable second-order continuous-time $\Delta \Sigma$ A/D converter, the power consumption of the third-order continuous-time $\Delta \Sigma$ A/D converter decreases with decreasing the reference-currents, and the clock frequency, but the energy consumption per sample increases, because the oversampling ratio and the number of clock cycles required for a single sample do not change with the programmability of the A/D converter.
5.1 Introduction

In the pursuit of an RF-powered programmable A/D converter design, multiple chips were designed and fabricated: a programmable continuous-time second-order ΔΣ A/D converter using MOSIS AMI 1.5 µm CMOS process, and an RF-power rectifier, a programmable continuous-time third-order ΔΣ A/D converter, and an RF-powered programmable continuous-time third-order ΔΣ A/D converter using MOSIS AMI 0.5 µm CMOS process. The wire-bonded micrographs of the fabricated chips are shown in the Appendices C.2, C.1, C.3, and C.4.

Test results for the programmable continuous-time second-order ΔΣ A/D converter and the RF-power rectifier chips are reported in this chapter. Testing of the RF-powered continuous-time third-order ΔΣ A/D converter is a future work.

5.2 Test Setup

Test setup for the programmable continuous-time ΔΣ A/D converter is shown in Fig. 5.1. A/D converter bias-currents and bias-voltages are generated externally.
with Keithley 236, 238 source-measurement-units and Keithley 4200 semiconductor characterization system. An external-clock for the A/D converter was generated with TLA7016 (TLA7PG2) 64-channel pattern-generator. The ∆Σ A/D converter single-bit output-stream was triggered and recorded with TLA7016 (TLA7NA2) 68-channel logic analyzer. Tektronix TDS5104B oscilloscope is used for the on-chip oscillator jitter measurements, and the A/D converter output rise and fall-times measurements.

Fig. 5.1. Test setup for the programmable continuous-time ∆Σ A/D converter.

Test setup for the RF-powered programmable continuous-time ∆Σ A/D converter is shown in Fig. 5.2. RF-power is applied to the RF-powered ∆Σ A/D converter with, directly connected to the on-chip RF-power rectifier, Agilent HP8360L synthesized swept-CW generator.

5.3 Programmable Continuous-Time Second-Order ∆Σ A/D Converter Test-Results

To test the programmable continuous-time second-order ∆Σ A/D converter, its reference-currents and the clock frequency must be set in accordance with their design values. Scaling the reference-currents and the clock-frequency simultaneously, and
by the same scaling factor, does not change the performance of the continuous-time ΔΣ A/D converter, in principle. Scaling gives an additional degree of freedom in choosing the reference-currents and the clock-frequency, that can be scaled to match different-application requirements, or to accommodate the process-variations of the transistor-parameters of the fabricated CMOS-chip.

Another method that is used to improve the dynamic-range of the ΔΣ A/D converter is called dynamic-scaling. Dynamic-scaling of the ΔΣ A/D converter reference-currents is independent of the clock-frequency, and is different from the simultaneous-scaling of these parameters. Dynamic-scaling of the ΔΣ A/D converter decreases the voltage variation on the integrating-capacitors, and therefore decreases the linearity-errors, and the errors due to finite output-resistances of the feedback-currents of the continuous-time ΔΣ A/D converter. Dynamic-scaling of the continuous-time ΔΣ A/D converter reference-currents is necessary in testing, due to the the post-
fabrication process-variations of the integration-capacitor values, by as much as 20%.

The programmable continuous-time second-order $\Delta \Sigma$ A/D converter reference-currents and clock-frequency are initially evaluated based on a model discrete-time second-order $\Delta \Sigma$ A/D converter feedback-coefficients. The discrete-time $\Delta \Sigma$ A/D converter feedback-coefficients are set to $a_1 = 0.4179$ and $a_2 = 1.0990$, for all test-results in this chapter. The feedback-coefficients, $a_1 = 0.4179$ and $a_2 = 1.0990$, are chosen, in return, so that the lowpass noise-transfer-function (NTF) of the discrete-time $\Delta \Sigma$ modulator achieves a quantization noise-suppression in the signal-band, that results in 12-bit A/D converter resolution, for the oversampling ratio $\text{OSR} = 1024$.

Testing of the continuous-time $\Delta \Sigma$ A/D converter is based on the fast Fourier transform (FFT) of the A/D converter single-bit output-stream. The FFT of the A/D converter output is used to estimate the signal to in-band noise power (SNR), the total harmonic distortion (THD), and the effective number of bits (ENOB). The FFT of the A/D converter output is valid only when the output data is rich in binary transitions. All FFT test-results are based on 130,000 output bits of the $\Delta \Sigma$ A/D converter. The differential non-linearity (DNL) and the integral non-linearity (INL) of the programmable second-order $\Delta \Sigma$ A/D were not measured due to our equipment limitations.

Initially, the continuous-time $\Delta \Sigma$ A/D converter was tested with high clock frequencies, to estimate the maximum allowable clock frequency. The reference-currents and the clock-frequency of the A/D converter are calculated based on their dynamically and synchronously-scaled continuous-time $\Delta \Sigma$ A/D converter-model parame-
ters. The test-parameters of the A/D converter for the clock frequency of $F_s = 4$ MHz are shown in Table 5.1, and the FFT of the A/D converter output is shown in Fig. 5.3. FFT of the continuous-time $\Delta \Sigma$ A/D converter output follows the noise-transfer-function (NTF) of the discrete-time $\Delta \Sigma$ A/D converter model at high-frequencies. Note that the x-scale is of the FFT plot is normalized to discrete-time frequency $\Omega = 1$. At low-frequencies, white noise dominates the output. The input currents to the $\Delta \Sigma$ A/D converter decrease from $1.74 \, \mu A$, in setting 1, to $6.8 \, nA$, in setting 2, where setting 1 and setting 2 are the two programmable states of the A/D converter.

Table 5.1. Programmable second-order $\Delta \Sigma$ A/D test parameters for $F_s = 4$ MHz.

<table>
<thead>
<tr>
<th></th>
<th>Setting 1</th>
<th>Setting 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F_s$</td>
<td>4 MHz</td>
<td>15.6 kHz</td>
</tr>
<tr>
<td>$I_{ref1}$</td>
<td>3.5 $\mu A$</td>
<td>13.7 $nA$</td>
</tr>
<tr>
<td>$I_{ref2}$</td>
<td>2.8 $\mu A$</td>
<td>10.9 $nA$</td>
</tr>
<tr>
<td>$G_{m1}$</td>
<td>16 $\mu A/V$</td>
<td>62.5 $nA/V$</td>
</tr>
<tr>
<td>$I_{amp}$</td>
<td>5 $\mu A$</td>
<td>19.5 $nA$</td>
</tr>
</tbody>
</table>

With high clock frequency, multiple factors influence the degradation of the continuous-time $\Delta \Sigma$ A/D converter performance. Compared to small clock period comparator’s and current feedback D/A converter’s rise and fall times become significant. Current feedback D/A converter’s settling time becomes more important as well. High white noise floor is partially due to the source noise as well.

To improve the continuous-time $\Delta \Sigma$ A/D converter performance, the clock frequency was decreased from 4 MHz to 1 MHz. The second-order $\Delta \Sigma$ A/D converter reference-currents and the amplifier bias currents, for the clock-frequencies of 1 MHz, in setting 1, and 3.9 kHz, in setting 2, are shown in Table 5.2. Decreasing the reference-currents, from setting 1 to setting 2 of the programmable A/D converter, is accomplished with programmable current D/A converters.
Fig. 5.3. Programmable continuous-time second-order $\Delta\Sigma$ A/D converter test at $F_s = 4$ MHz clock frequency and with current input.

Table 5.2. Programmable second-order $\Delta\Sigma$ A/D test parameters for $F_s = 1$ MHz.

<table>
<thead>
<tr>
<th>Setting</th>
<th>Setting 1</th>
<th>Setting 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F_s$</td>
<td>1 MHz</td>
<td>3.9 kHz</td>
</tr>
<tr>
<td>$I_{ref1}$</td>
<td>4.4 $\mu$A</td>
<td>17.2 nA</td>
</tr>
<tr>
<td>$I_{ref2}$</td>
<td>3.5 $\mu$A</td>
<td>13.7 nA</td>
</tr>
<tr>
<td>$G_{m1}$</td>
<td>16 $\mu$A/V</td>
<td>62.5 nA/V</td>
</tr>
<tr>
<td>$I_{amp}$</td>
<td>0.8 $\mu$A</td>
<td>3.1 nA</td>
</tr>
</tbody>
</table>
The programmable continuous-time second-order ΔΣ A/D converter was tested with the reference-currents and the clock-frequencies shown in Table 5.2. The fast-Fourier-transforms (FFT) of the A/D converter outputs, when the input-current is equal to $I_{in} = 1.7 \mu A$ or -8.3 dB, in setting 1, and to $I_{in} = 10.2 \, nA$ or -4.5 dB, in setting 2, are shown in Fig. 5.4. The noise floor decreases by 20dB compared to the case of higher clock-frequency, $F_s = MHz$. Test results for different input-currents, $I_{in} = 1 \, \mu A$ or -12.8 dB, in setting 1, and $I_{in} = 0.7 \, nA$ or -27.8 dB, in setting 2, are shown in Fig. 5.5. Note that the input-current cannot be decreased arbitrarily. There must be significant number of 0-1 and 1-0 transitions in the output bit-sequence of the ΔΣ modulator for the FFT to be meaningful.

Fig. 5.4. Programmable continuous-time second-order ΔΣ A/D converter test FFT for $F_s = 4 \, MHz$ and with current input 1.
Programmable A/D converter performance was also tested with light-input conditions. The light was generated using a green LED, connected to a current-source. It was noted, that for ultra-low input-light conditions, the noise-shaping curve tends to deviate from an ideal, whereas for ultra-high input-light conditions the noise-shaping curve changes from a second-order into a first-order, due to slewing of the amplifier. Testing with light was also conducted with 1 MHz clock frequency and using the same reference currents as in Table 5.2. When testing with light-input, the photo-diode current is estimated by measuring its mirrored-value with the input-buffer. FFTs of the A/D converter output for the first test-set, with a light-input, and measured
photo-detector currents of $I_{PD} = 1.03 \mu A$ or -12.6 dB, in setting 1, and $I_{PD} = 1.34 \text{ nA}$ or -22.2 dB, in setting 2, are shown in Fig. 5.6. FFTs of the A/D converter output for a different test-set, with photo-detector currents of $I_{PD} = 663 \text{ nA}$ or -16.4 dB, in setting 1, and $I_{PD} = 1.34 \text{ nA}$ or -22.2 dB, in setting 2, are shown in Fig. 5.7.

![Delta-sigma ADC Test Data FFT - Light Input](image)

**Fig. 5.6.** Programmable continuous-time second-order $\Delta\Sigma$ A/D converter FFT test for $F_s = 1 \text{ MHz}$ and light input 1.

A few problems are worth mentioning, that motivated the design of a programmable third-order continuous-time $\Delta\Sigma$ A/D converter using a new architecture. When the input-currents to the A/D converter are ultra-low, i.e. 500 pA, the feedback-network of the input-buffer oscillates. Hspice simulations verify that with low input-currents the negative-feedback of the input-buffer is unstable. Therefore, in the next design,
The input-buffer was eliminated.

Because rigorous INL (integral non-linearity) and DNL (differential non-linearity) tests of ΔΣ A/D converter were not possible due to our equipment limitations, it was still possible to test the A/D converter linearity with two series of tests. One was a sweep of the input-current, shown in Fig. 5.8, and the other was a sweep of input-light, shown in Fig. 5.9. Both tests were conducted with lowest reference-currents, and clock-frequencies possible of the programmable continuous-time ΔΣ A/D converter.
The A/D converter power-consumption tests are shown in Table 5.3. The power-consumption measurement includes the reference-current D/A converter, and the A/D converter single-bit quantizer supply-currents. The single-bit quantizer consumes a constant 60 $\mu$A supply-current, that does not scale with programmability.

Table 5.3. Programmable A/D power test with different D/A settings.

<table>
<thead>
<tr>
<th>Setting</th>
<th>IBIAS$_{ADC}$</th>
<th>FREQ</th>
<th>$I_{VDD}$</th>
<th>$P_{VDD}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Setting 1</td>
<td>4.4 $\mu$A</td>
<td>1 MHz</td>
<td>86.8 $\mu$A</td>
<td>434 $\mu$W</td>
</tr>
<tr>
<td>Setting 2</td>
<td>:4</td>
<td>225 kHz</td>
<td>71 $\mu$A</td>
<td>355 $\mu$W</td>
</tr>
<tr>
<td>Setting 3</td>
<td>:16</td>
<td>56 kHz</td>
<td>66.8 $\mu$A</td>
<td>334 $\mu$W</td>
</tr>
<tr>
<td>Setting 4</td>
<td>:64</td>
<td>14 kHz</td>
<td>65.2 $\mu$A</td>
<td>326 $\mu$W</td>
</tr>
<tr>
<td>Setting 5</td>
<td>:256</td>
<td>3.5 kHz</td>
<td>65 $\mu$A</td>
<td>325 $\mu$W</td>
</tr>
</tbody>
</table>
Fig. 5.9. Second order ∆Σ A/D converter test with a photo-diode current sweep.

The on-chip oscillator frequency and power test-results are shown in Table 5.4. The current-controlled ring-oscillator supply-current measurements are much higher than what Hspice simulations predicted. The increase in oscillator power is the result of high loading capacitances, compared to 100 fF, assumed in Hspice simulations.

Table 5.4. Current controlled oscillator power and frequency vs bias current test.

<table>
<thead>
<tr>
<th>Setting</th>
<th>$I_{BIAS_{OSC}}$</th>
<th>FREQ</th>
<th>$I_{VDD}$</th>
<th>$P_{VDD}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Setting 1</td>
<td>19.2 µA</td>
<td>1.06 MHz</td>
<td>175.5 µA</td>
<td>877.5 µW</td>
</tr>
<tr>
<td>Setting 2</td>
<td>4.9 µA</td>
<td>229 kHz</td>
<td>71 µA</td>
<td>355 µW</td>
</tr>
<tr>
<td>Setting 3</td>
<td>1.3 µA</td>
<td>56.7 kHz</td>
<td>43 µA</td>
<td>215 µW</td>
</tr>
<tr>
<td>Setting 4</td>
<td>333 nA</td>
<td>13.8 kHz</td>
<td>37.3 µA</td>
<td>186.5 µW</td>
</tr>
<tr>
<td>Setting 5</td>
<td>95 nA</td>
<td>3.8 kHz</td>
<td>36 µA</td>
<td>180 µW</td>
</tr>
</tbody>
</table>
5.4 RF-Power Rectifier Test Results

Two-versions of an RF-power rectifier was fabricated: using diode-connected MOS transistors, and Schottky diodes, available in MOSIS ON 0.5 μm process. The test-results of the power-rectifiers, shown in Table 5.5 and Table 5.6, indicate Schottky diode out-performs the MOSFET-based rectifier, due to its lower turn-on voltage. Both RF-power rectifier tests were conducted under no-load conditions, but their DC-voltage outputs were easily driving an LED to its full brightness.

Table 5.5. MOS-based RF power rectifier test.

<table>
<thead>
<tr>
<th>FREQ</th>
<th>RF-POWER</th>
<th>VDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>305 MHz</td>
<td>0 dBm</td>
<td>1.2 V</td>
</tr>
<tr>
<td>302 MHz</td>
<td>3 dBm</td>
<td>2.8 V</td>
</tr>
<tr>
<td>305 MHz</td>
<td>5 dBm</td>
<td>4.2 V</td>
</tr>
</tbody>
</table>

Table 5.6. Schottky-based RF power rectifier test.

<table>
<thead>
<tr>
<th>FREQ</th>
<th>RF-POWER</th>
<th>VDD</th>
</tr>
</thead>
<tbody>
<tr>
<td>348 MHz</td>
<td>-10 dBm</td>
<td>1 V</td>
</tr>
<tr>
<td>258 MHz</td>
<td>0 dBm</td>
<td>3.6 V</td>
</tr>
<tr>
<td>269 MHz</td>
<td>3 dBm</td>
<td>5.3 V</td>
</tr>
<tr>
<td>317 MHz</td>
<td>5 dBm</td>
<td>6.8 V</td>
</tr>
</tbody>
</table>

5.5 Summary

The programmable second-order continuous-time ΔΣ A/D converter was fully tested and characterized. The A/D converter achieves a 17 to 20-bit dynamic-range with a programmable 8-12 bit ΔΣ A/D converter. Programming the reference-currents of the ΔΣ A/D converter, requires a simultaneous programming of the clock-frequency. And programming the clock-frequency results in a significant on-chip oscillator power-savings. Decreasing the frequency of the oscillator from 1 MHz to 3.8 kHz, i.e. ratio of 264, the oscillator power decreases from 175 μA to 36 μA, i.e. ratio of 4.9. The supply-current of the A/D converter does not change with
programmability, and is equal, approximately, to 60 µA. The A/D converter power-consumption is higher than in simulations, because the parasitic load-capacitances at the output of the A/D converter are significantly higher than the assumed loading-capacitance value of 100 fF.
Conclusions and Future Work

6.1 Programmable Continuous-Time Second-Order $\Delta\Sigma$ A/D Converter in 1.5 $\mu$m CMOS

A programmable second-order continuous-time $\Delta\Sigma$ A/D converter was designed and fabricated using MOSIS AMI 1.5 $\mu$m 5-V CMOS-process. The test results indicate that the programmable A/D converter achieves a wide-dynamic-range of 20-bits by decreasing the reference-currents from 4.4 $\mu$A to 17.2 nA, and, simultaneously, decreasing the clock-frequency and the sample-rate from 1 kSamples/s to 3.8 Samples/s. The power-consumption of the A/D converter, during testing, decreases from 900 $\mu$W to 200 $\mu$W, with a 5 V supply-voltage.

The table comparing this work to low-power wide-dynamic-range A/D converters, available in the literature, are shown in Table 6.1. The A/D converters in this table are limited only to current-input A/D converters, suitable for photo-detector based applications.
Table 6.1. Low-Power Wide-Dynamic-Range A/D Converters Comparison-Table.

<table>
<thead>
<tr>
<th></th>
<th>Resolution</th>
<th>Power</th>
<th>Supply-Voltage</th>
<th>Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADI ADAS1128</td>
<td>24 bits</td>
<td>4.5 mW</td>
<td>3.3 V</td>
<td>-</td>
</tr>
<tr>
<td>TI DDC118</td>
<td>20 bits</td>
<td>13.5 mW</td>
<td>5 V</td>
<td>-</td>
</tr>
<tr>
<td>[39]</td>
<td>13 bits</td>
<td>210 µW</td>
<td>2.2 V</td>
<td>0.5 µm CMOS</td>
</tr>
<tr>
<td>[16]</td>
<td>13 bits</td>
<td>-</td>
<td>1 V</td>
<td>0.18 µm CMOS</td>
</tr>
<tr>
<td>[31]</td>
<td>12 bits</td>
<td>7.7 mW</td>
<td>5 V</td>
<td>0.7 µm CMOS</td>
</tr>
<tr>
<td>[41]</td>
<td>8 bits</td>
<td>1.8 µW</td>
<td>1 V</td>
<td>0.25 µm CMOS</td>
</tr>
<tr>
<td>[35]</td>
<td>8 bits</td>
<td>3.1 µW</td>
<td>1 V</td>
<td>0.25 µm CMOS</td>
</tr>
<tr>
<td>[40]</td>
<td>12 bits</td>
<td>25 µW</td>
<td>1 V</td>
<td>0.18 µm CMOS</td>
</tr>
<tr>
<td>This Work</td>
<td>20 bits</td>
<td>900 µW</td>
<td>5 V</td>
<td>1.5 µm CMOS</td>
</tr>
</tbody>
</table>

The A/D converter achieves high-resolution, 20-bits, with only 900 µW power-consumption and 5 V supply voltage.

6.2 RF-Powered Programmable Continuous-Time Third-Order ∆Σ A/D Converter in 0.5 µm CMOS

An RF-powered programmable continuous-time third-order ∆Σ A/D converter is designed and fabricated using MOSIS ON 0.5 µm 3-V CMOS process. It is designed to achieve a 20-bit dynamic-range with an oversampling ratio of only 128. All on-chip components, i.e. the voltage regulator, the bandgap voltage-reference circuit, the beta-multiplier current-reference circuit, the continuous-time third-order ∆Σ A/D converter, and the on-chip five-stage current-controlled ring-oscillator are designed to consume less than 40 µA of current with the supply-voltage of 3 V. Decreasing the reference-currents, and the clock-frequency of the A/D converter decreases the power-consumption of the system from 120 µW to 60 µW, whereas the sample-rate decreases from 11.2 kSamples/s to 142 Samples/s.

Testing of the RF-powered A/D converter is a future work. Comparison table of the design specifications of the RF-powered programmable continuous-time third-order ∆Σ A/D converter with, available in the literature, RF-powered sensor systems
is shown in Table 6.2.

Table 6.2. Passive RFID Tags-with-Sensors Comparison-Table.

<table>
<thead>
<tr>
<th></th>
<th>Frequency</th>
<th>Power</th>
<th>Supply-Voltage</th>
<th>Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>[12]</td>
<td>960 MHz</td>
<td>5.14 µW</td>
<td>1.5 V</td>
<td>0.25 µm CMOS</td>
</tr>
<tr>
<td>[25]</td>
<td>970 MHz</td>
<td>16.7 µW</td>
<td>1.5 V</td>
<td>0.5 µm CMOS</td>
</tr>
<tr>
<td>[21]</td>
<td>915 MHz</td>
<td>14.4 µW</td>
<td>1.2 V</td>
<td>0.5 µm CMOS</td>
</tr>
<tr>
<td>[46]</td>
<td>900 MHz</td>
<td>1.5 µW</td>
<td>1.5 V</td>
<td>0.18 µm CMOS</td>
</tr>
<tr>
<td>This Work</td>
<td>350 MHz</td>
<td>120 µW</td>
<td>3 V</td>
<td>0.5 µm CMOS</td>
</tr>
</tbody>
</table>

The proposed RF-powered sensor system consumes large power, 120 µW, because of its high-supply voltage, 3 V, and the medium-to-high resolution on-chip A/D converter, 12 - 20 bits.
Appendix A

Programmable Continuous-Time Second-Order $\Delta\Sigma$ A/D Converter Chip Component-Layouts in 1.5 $\mu$m CMOS

A.1 Current-Feedback D/A Converter Layout

Fig. A.1. Current-feedback D/A converter layout.
A.2 Input-Current Buffer Layout

Fig. A.2. Input-current buffer layout.
A.3 Operational Transconductance Amplifier Layout

Fig. A.3. Operational transconductance amplifier layout.
A.4 Programmable Current-Reference D/A Converter Layout

Fig. A.4. Programmable current-reference D/A converter layout.
A.5 Three-Stage Current-Controlled Ring-Oscillator Layout

Fig. A.5. Three-stage current-controlled ring-oscillator layout.
Appendix B

RF-Powered Programmable Continuous-Time Third-Order ΔΣ A/D Converter Chip Component-Layouts in 0.5 μm CMOS

B.1 RF-Power Rectifier Layout

Fig. B.1. RF-power rectifier layout.
B.2 Voltage-Limiter Layout

Fig. B.2. Voltage-limiter layout.
B.3 Linear Shunt Voltage-Regulator Layout

Fig. B.3. Linear shunt voltage-regulator layout.
B.4 Bandgap Voltage-Reference Circuit Layout

Fig. B.4. Bandgap voltage-reference circuit layout.
B.5 Beta-Multiplier Current-Reference Circuit Layout

Fig. B.5. Beta-multiplier current-reference circuit layout.
Fig. B.6. Programmable current-reference D/A converter layout.
B.7 Five-Stage Current-Controlled Ring-Oscillator Layout

Fig. B.7. Five-stage current-controlled ring-oscillator layout.
B.8 Operational Transconductance Amplifier Layout

Fig. B.8. Operational transconductance amplifier layout.
Appendix C

Chip Micrographs

C.1 RF-Power Rectifier Micrograph in 0.5 µm CMOS

Fig. C.1. RF-power rectifier micrograph in 0.5 µm CMOS.
C.2 Programmable Continuous-Time Second-Order A/D Converter Micrograph in 1.5 $\mu$m CMOS

Fig. C.2. Programmable continuous-time second-order $\Delta\Sigma$ A/D converter micrograph in 1.5 $\mu$m CMOS.
C.3 Programmable Continuous-Time Third-Order $\Delta \Sigma$ A/D Converter Micrograph in 0.5 $\mu$m CMOS

Fig. C.3. Programmable continuous-time third-order $\Delta \Sigma$ A/D converter micrograph in 0.5 $\mu$m CMOS.
C.4 RF-Powered Programmable Continuous-Time Third-Order ∆Σ A/D Converter Micrograph in 0.5 µm CMOS

Fig. C.4. RF-powered programmable continuous-time third-order ∆Σ A/D converter micrograph in 0.5 µm CMOS.
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Biography

Arnak Aleksanyan was born in Yerevan, Armenia on February 27, 1976. He received his Bachelor of Science degree in Radio-Physics from Yerevan State University in 1998 and Master of Science in Electrical Engineering degree from University of Southern California, Los Angeles, CA in 2004. He was enrolled in Ph. D. program in Electrical Engineering at Duke University since September, 2005.