

Low-Frequency Scheduler for Optimal Conduction Loss in Series/Parallel Modular Multilevel Converters

Nima Tashakor, *Student Member, IEEE*, Farzad Iraj, and Stefan Goetz, *Member, IEEE*

Abstract—Various advantages are directing the attention to modular multilevel converters (MMCs). Simple ways to balance the voltage difference of MMC modules are strongly desired but an open problem. The modular multilevel series/parallel converter (MMSPC) can be an efficient solution for this problem. However, implementing an effective control method is essential for close-to-optimum operation of MMSPCs. Generally, on the higher level of control, various modulation techniques can control the output, while a scheduler balances the module voltages on a lower control level. This paper proposes a simple yet powerful module scheduling method for MMSPCs. This scheduling method can be combined with many modulation techniques, such as nearest-level modulation (NLM). It reduces the control complexity using the sensorless balancing capability, improves efficiency by minimizing the conduction loss, and achieves a compromise between balancing the module voltages and switching loss. Though applicable to other modulation methods, simulation and experiments combine the proposed method with NLM for a comparison with the prior art of scheduling. Based on the presented results and analysis, the algorithm is suited particularly for MMSPCs with a low to medium number of modules. The proposed technique achieves 18–55% reduction in power loss and 7.5% improvement in averaged capacitor currents compared to other algorithms.

Index Terms—Capacitor voltage balancing, modulation technique, modular multilevel converter (MMC), modular multilevel series/parallel converter (MMSPC).

I. INTRODUCTION

A number of advantages such as lower voltage stress on module components, improved harmonic performance, and high reliability are key features of multilevel converters [1], [2]. The modular multilevel converter (MMC) is the most performant topology family for medium- to high-voltage applications [3]–[5]. Their scalability which allows reaching practically any high voltage level with low-voltage sub-modules (SMs) is the main appeal of MMCs [6].

In the past years, various topologies for MMCs and their modules have been proposed, such as half-bridge [7], full-bridge [8], clamp-double [9], and three-level modules [10]. Without actively balancing, inherent mismatches between modules caused either by parameter spread or different leakage and aging speeds are the main reasons for capacitor voltage imbalance [11], [12]. Proper topologies [13], [14] and/or control methods [11], [15]–[17] can solve this issue. Control methods for balancing require voltage and/or current measurements for each module, which increase the overall system cost as well as complexity [18], [19]. Such requirements and the high software involvement are the reasons that MMCs have

issues in applications that require safety integrity level (SIL) ratings. Thus topologies that allow simpler or even hardware-ensured balancing are an attractive alternative. The modular multilevel series/parallel converter (MMSPC) is a modified MMC topology that introduces a parallel functionality on top of the serial connection [20]–[23]. Among other advantages, MMSPC with its extra parallel connection across modules can prevent voltage imbalance by frequently connecting neighboring modules in parallel [24]. The temporary parallel connection of two or more modules leads to balancing of module voltages similar as in switched-capacitor circuits [25]. Due to MMSPC's intrinsic balancing capability, the requirement for voltage and current sensors is released [26], [27].

Conventional MMCs require a strategy to actively balance and maintain capacitor voltages within a reasonable boundary [28]–[30]. Sorting is the dominant method for balancing the module voltages [31], [32], where modules with highest voltage are inserted in series first when the arm current is negative or last if the arm current is positive and vice versa [18], [33]–[36]. The main problem of methods based on cell sorting is the need to measure the module voltages, which leads to higher cost, or estimate them, which complicates algorithms and can reduce reliability.

Although different modulation and scheduling techniques for enhancing the performance of conventional MMCs are available, few of them, such as [37] and [38], focus on systematically improving MMSPC's performance. Since MMSPC modules offer bypass, serial, and parallel connections, of which MMC is a subset, all conventional MMC modes and scheduling methods in principle work for MMSPC. Preferably parallel replaces bypass states for lower conduction loss and switched-capacitor balancing. However, there are some fine intrinsic differences that allow increasing the performance if exploited. As will be shown in Section IV, the order by which serial/parallel connections are assigned to modules throughout the arm affects the effective impedance and loss [39]. The conventional MMC's equivalent resistance, in contrast, only depends on the number of serial/bypass connections and not their assignment order in the arm [40], [41].

This paper proposes a scheduling method for MMSPC topologies that also works with fundamental-frequency switching and can be readily combined with most modulation techniques. After determining the required arm voltage level by the modulator, the proposed method achieves minimum conduction loss by minimizing the equivalent resistance of the arm. Additionally, while the parallel functionality allows

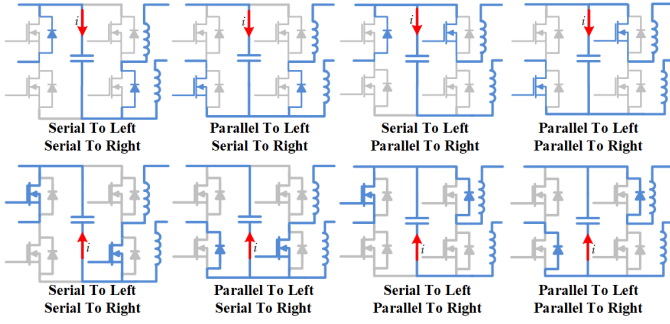


Fig. 1. Different switching conditions which is used in the proposed method.

voltage balancing, the proposed method further reduces the accumulated imbalance when there are multiple choices for a specific minimum equivalent resistance. Finally, to reduce the switching loss, PWM is avoided. The proposed method with MMSPC topology is especially effective in high-power applications with medium to high frequency output voltages, where high currents and fast responses are of importance. The main contributions of the paper are as follows:

- 1) Minimization of the conduction loss with comparable THD values.
- 2) Maintenance of a sensorless scheduling method that reduces the costs and simplifies the system.
- 3) Better voltage balancing and current sharing among modules even compared to cell sorting technique.
- 4) Applicability to a wide range of modulation techniques.

II. PRINCIPLE OPERATION AND ANALYSIS

The three major topologies for MMSPC are semi full-bridge [42], full-bridge [43], and dual full-bridge [44]. The following describes the proposed algorithm, which is capable of handling all the above-mentioned module topologies. For the sake of clarity, the operation principle and analysis use the full-bridge topology, while it can easily be transferred to other topologies with parallel mode [45].

In the considered MMSPC, two identical arms, each including N modules, form a phase and the number of phases can be arbitrary. Except for the last module in each arm, every module incorporates a dual half-bridge topology. One half-bridge controls the module connection to the upper and the other half-bridge controls the connection to lower modules. Such an arrangement results in eight different conditions for each module with respect to the arm current direction, illustrated in Fig. 1 for positive and negative currents. Configuring modules in parallel equalizes the capacitor voltages. With a very low resistance path, current spikes are a common challenge but can be easily solved by small inductors [14], [46].

Fig. 2 shows the circuit diagram of a single-phase MMSPC system. The larger inductor (L_{arm}) in series with each arm limits surge currents due to voltage difference between the dc link and the arms. Parallel connection of an arbitrary number of phases to the dc link can form a multi-phase system. In a multi-phase system, the arm inductor is also responsible for limiting the circulating current between the phases.

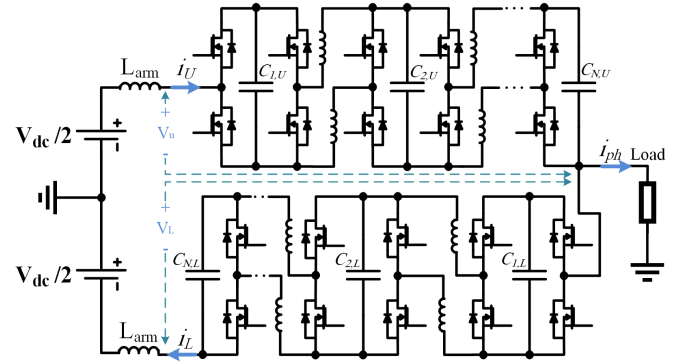


Fig. 2. Circuit diagram of a single-phase MMSPC.

A. Analysis of the MMSPC from Load Perspective

From the output perspective, any number of modules connected in parallel (called a parallel union or short union) are considered as one, and they contribute to the output voltage identical to a single series module. Therefore, all the MMC analysis holds [47]. Considering arm voltages continuous, Kirchoff's law for steady state conditions follows

$$v_{ph} = -v_U - L \frac{di_U}{dt} - R i_U + \frac{V_{dc}}{2}, \quad (1)$$

$$v_{ph} = -v_L + L \frac{di_L}{dt} + R i_L + \frac{V_{dc}}{2},$$

$$i_{ph} = i_U - i_L,$$

where (u_{ph}, i_{ph}) , (v_U, i_U) , and (v_L, i_L) are voltages and currents of the phase, upper arm, and lower arm, respectively. The equivalent resistance of the arm is derived with more detail in Section IV, but (2) provides an approximation for a more general analysis of the system as

$$R = R_{arm} + \frac{N-1}{2} R_{SW}, \quad (2)$$

where R_{SW} is the switch resistance of module. The equivalent inductance of the arm (L) can be calculated per

$$L = L_{arm} + \frac{N-1}{2} L_{SM}. \quad (3)$$

where L_{SM} is the small inductance between two side-by-side module and should be calculated using (4) to ensure proper performance of the system [48].

$$L_{SM} = \min \left(\left[\left(\frac{V_{diff,max}}{i_{rated}} + \frac{R_e}{2} \right)^2 + \frac{R_e^2}{4} \right] C_e, \frac{V_{diff,max} \times T_s}{i_{rated}} \right), \quad (4)$$

where $V_{diff,max}$ is maximum voltage difference between modules, i_{rated} is rated current of the switch, R_e and C_e are simplified circuit parameters as detailed in the literature [48]. The calculation procedure for selecting suitable module capacitors is proposed by Merlin et al. [49]. The final equation follows

$$C_{SM} \geq \frac{|S|}{6\pi f_1} \frac{1}{V_{DC} \Delta V}, \quad (5)$$

where S is apparent power of the MMC system, f_1 is output frequency, and ΔV is maximum allowable capacitor voltage drop.

A proper configuration to meet the specified voltage level is the main objective of the modulation method. Most of the modulation methods proposed in the literature quantize voltage references into discrete voltage levels and determine the number of series modules/unions. The scheduler, including the proposed one, takes over right after the modulator has determined the number of required serial connections (N_s) and uses N_s as input to determine the optimized connection of the modules. This structure renders the proposed method applicable to nearest-level modulation (NLM) methods and any other switching method that controls N_s directly [50]. Since NLM can achieve lower THDs with less switching, this paper studies the proposed scheduler in detail using NLM. However, since the only input of the proposed scheduler is the number of required serial connections, it can be easily combined with other modulation techniques too.

Using (1), the phase output voltage can be calculated as

$$v_{ph} = \frac{1}{2}(v_L - v_U + L \frac{di_{ph}}{dt} + R i_{ph}). \quad (6)$$

The voltage reference for the phase can be derived as

$$v_{ref} = \frac{1}{2} m V_{dc} \cos(\omega t), \quad (7)$$

where m is the modulation index. Similarly, upper and lower reference voltages can be expressed as

$$v_{ref}^U = \frac{1}{2} V_{dc}(1 - m \cos(\omega t)), \quad (8)$$

$$v_{ref}^L = \frac{1}{2} V_{dc}(1 + m \cos(\omega t)),$$

where ω is angular velocity of the fundamental frequency of the output voltage of the MMSPC. In conventional NLM (CNLM) methods, the upper and lower arms should be switched complementary, which results in $N + 1$ different voltage levels. The quantized voltage levels could be produced by changing series modules. Furthermore, applying a $\pi/2N$ phase shift between switching of the upper and lower arms enables $2N + 1$ voltage levels. This paper refers to this method as phase-shifted arms NLM (PSANLM). A larger number of voltage levels improves the output THD and reduces the capacitors voltage from $\frac{V_{dc}}{2N}$ to $\frac{V_{dc}}{2N+1}$. The N_s for PSANLM can be calculated as

$$\begin{aligned} N_{SU} &= \text{round} \left(\frac{N v_{ref}^U}{V_{dc}} + \frac{1}{4} \right), \\ N_{SL} &= \text{round} \left(\frac{N v_{ref}^L}{V_{dc}} + \frac{1}{4} \right). \end{aligned} \quad (9)$$

B. System Priorities

1) *Conduction Loss*: This parameter is influenced by the number of series/parallel modules as well as their mapping throughout the arm. Assuming modules are identical and capacitor voltages are balanced, the conduction loss is quadratically related to the arm equivalent impedance. To minimize conduction loss, the system's equivalent impedance should be minimized. To minimize the impedance for a given N_s , it is

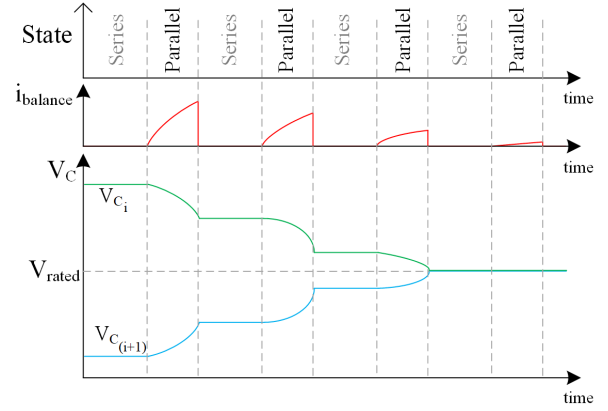


Fig. 3. Representative voltage and current waveforms during balancing.

proven that all the unions should have a similar number of parallel modules and thus be as close as possible to a uniform distribution [38], [51]. In other words, a better distribution of parallel modules in each arm leads to lower equivalent resistance.

2) *Switching Loss*: The fewer modules change their connection state, the lower the switching loss. The proposed scheduler optimizes the conduction losses of the system, and hence it is particularly suitable for systems with high ratios of conduction to switching losses—in MMC applications, conduction losses typically contribute to a large portion of the overall losses. However, the algorithm limits the switching loss through low-frequency switching algorithms. The scheduler is effective for all systems with any number of modules, but the observed improvements are more noticeable in systems with fewer of modules. Additionally, the scheduler improves the balancing among modules, which is beneficial to both small and large systems.

3) *Charge Balancing*: The MMSPC topology can connect a module in parallel with another module, which simplifies the control system. Considering that one module has a lower voltage when connected in parallel, a balancing path will be formed and the module with the higher voltage will discharge into the one with the lower voltage, until their voltages are equal. However, since a parallel connection of two capacitors may lead to current spikes that can damage the components, very small inductors are used between modules to limit the balancing current amplitude. Therefore, depending on the imbalance existing between modules, balancing operation can take several cycles as depicted in Fig. 3.

While the scheduler's preferred course of action is to reduce the switching loss, when switching is necessary, the scheduler reduces imbalance by reversing the mapping order of the modules. In short, if two different unions with N_{p1} and N_{p2} parallel modules are required and the scheduler formed the unions for the previous voltage cycle starting from the upper module, the scheduler will start from the lower module in the arm in the next cycle.

III. PROPOSED CONTROLLER

Higher numbers of states for MMSPCs increase the degrees of freedom of the system. However, without solving a complex and time-consuming optimization problem for each time step, mathematically optimum operation cannot certainly be reached. The proposed method exploits the fine relations governing MMSPCs to solve the most important part of this optimization (minimizing loss), with consideration of other parameters. The main aim of the proposed controller is to minimize the power loss and since in high-power applications the larger share of power loss stems from conduction loss, it is reasonable to minimize the conduction loss first and reduce the switching loss second. As mentioned before, to minimize the conduction loss in each arm, the formed unions through paralleling the modules should be distributed as evenly as possible. Hence, for a specific N_s , the number of modules in each parallel unit of each arm (N_{p_i} , $i = 1, \dots, N_s$) should be equal or close to equal. To calculate every N_{p_i} , the value of $h = N/N_s$ should be considered, where N is the total number of modules in the arm. Depending on the value of h , two different conditions are possible:

1) h is a natural number: It means that N is an integer multiple of N_s . In this scenario, all N_{p_i} are equal to

$$N_{p_1} = N_{p_2} = \dots = N_{p(N_s)} = N/N_s. \quad (10)$$

2) h is not a natural number: There is a non-zero remainder (R) in the division. In this situation, R units should have $(\text{floor}(h) + 1)$ modules and $(N_s - R)$ units should have $\text{floor}(h)$ modules and these units are connected in a way that no similar units are connected in series to each other (for better balancing). Therefore, numbers of parallel modules in the two possible unions are

$$\begin{aligned} N_{p_1} = \dots = N_{p_R} &= \text{floor}(h) + 1, \\ N_{p(R+1)} = \dots = N_{p(N_s)} &= \text{floor}(h), \end{aligned} \quad (11)$$

where $f(x) = \text{floor}(x)$ is a function which yields the largest integer less than or equal to x as output. It should be mentioned that procedure is similar for positive and negative arm current and also for increase and decrease of N_s . The procedure is summarized as a flowchart in Fig. 4.

IV. THD AND LOSS DISCUSSION

Through analysis, this section derives the minimum equivalent resistance of the system and shows that the proposed scheduler has no adverse effect on the THD output.

A. Conduction Loss

Neglecting transients and voltage imbalance, the conduction loss can be estimated by equivalent resistance ($R_{\text{eq,arm}}$) and arm current. The equivalent resistive circuit of a union formed by N_{p_i} parallel modules is shown in Fig. 5 and the equivalent resistance of the union can be calculated using (12). Knowing N_s and the resultant N_{p_i} s, the equivalent resistance of the arm ($R_{\text{eq,arm}}$) could be calculated per

$$R_{\text{eq,union}} = \frac{R_C}{N_{p_i}} + \frac{N_{p_i} - 1}{2} (R_{L,\text{int}} + R_{\text{sw}}), \quad (12)$$

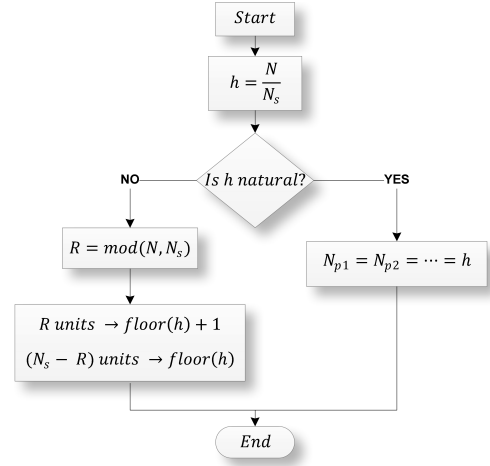


Fig. 4. Flowchart of the proposed scheduling algorithm.

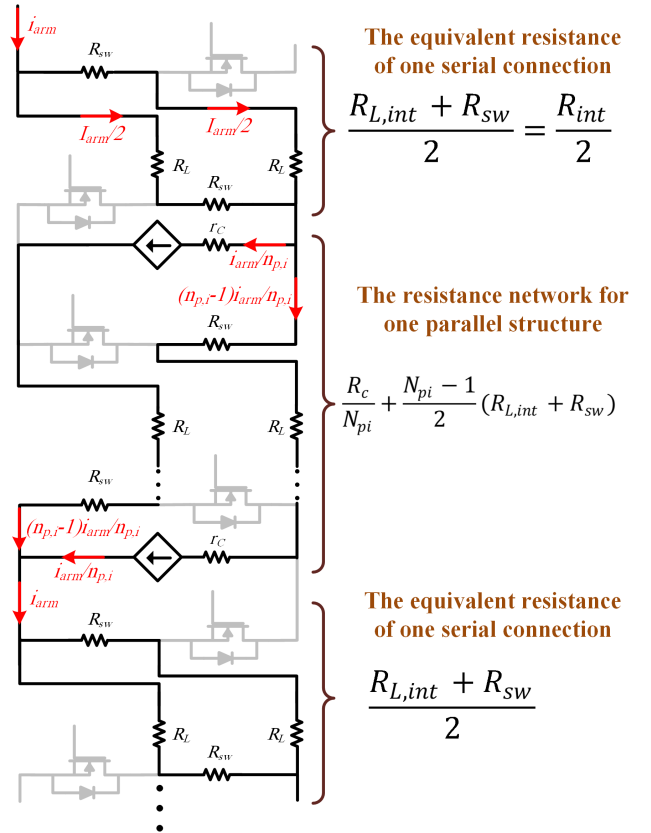


Fig. 5. Equivalent circuit of one union with N_{p_i} parallel modules.

$$\begin{aligned} R_{\text{eq,arm}} &= R_{L,\text{arm}} + \sum_{i=1}^{N_s} (R_{\text{eq,union}_i}) \\ &+ (N_s - 1) \left(\frac{R_{L,\text{int}} + R_{\text{sw}}}{2} \right) + R_{\text{sw}}, \end{aligned} \quad (13)$$

where R_C is internal resistance of capacitor, $R_{L,\text{int}}$ is internal resistance of the small inductance between modules, $R_{L,\text{arm}}$ is L_{arm} internal resistance, and R_{sw} is the switch resistance.

For conduction loss comparison of the proposed method with an MMC topology, the arm equivalent resistance should be calculated. Lets assume an MMC topology with half-bridge

modules, then the MMSPC has two times more individual switches compared to MMC because of parallel currents paths existence. Therefore, the effective current of MMSPC switches is half compared to a switch in an MMC that means smaller switches could be used in MMSPC [52]. For a fair comparison, the resistance of MMC switches is considered to be half the resistance of MMSPC ones. The equivalent arm resistance of a conventional MMC can be calculated as4

$$\begin{aligned} R_{\text{eq,arm}} &= R_{\text{L,arm}} + N_s r_c + N R_{\text{sw,MMC}} \\ &= R_{\text{L,arm}} + N_s r_c + N \frac{R_{\text{sw}}}{2}, \end{aligned} \quad (14)$$

where $R_{\text{L,arm}}$ is the main inductor resistance of the arm. The conventional MMC modules do not have parallel functionality, therefore the interconnection inductors between each module to decrease balancing current peak could be omitted, in other words, R_{sw} could represent the internal resistance as in (14).

Instantaneous arm current and the arm rms current can be calculated as

$$i_{\text{arm}} = \frac{I_{\text{ph}}}{2} \left(\frac{m}{2} \cos(\phi) \pm \sin(\omega t - \phi) \right), \quad (15)$$

$$I_{\text{arm}}^{\text{rms}} = \frac{I_{\text{ph}}}{2} \sqrt{\frac{m^2}{4} \cos^2(\phi) + \frac{1}{2}}, \quad (16)$$

where ϕ is the phase angle of load and I_{ph} is the phase current amplitude. The average model conduction loss can be calculated as the following [53]:

$$P_{\text{cond,arm}} = N V_{\text{CE}} I_{\text{arm}}^{\text{rms}} + R_{\text{eq,arm}} (I_{\text{arm}}^{\text{rms}})^2 \quad (17)$$

To reduce complexity in (17), forward voltages of anti-parallel diode and IGBT are considered equal. Besides, the forward voltages are assumed to be independent of current variations. The formulations show that the conduction loss due to the switches resistance is almost unchanged but the loss due to the capacitor resistance is reduced significantly. On the other hand, capacitors are operating in parallel so that the effective capacitance is increased, whereas each capacitor's effective current is reduced, enabling smaller capacitors.

B. Switching Loss

In case of completely balanced modules, the switching loss can be calculated based on the procedure proposed in [54]. To estimate the system switching loss, it is necessary to approximate the total number of switching instances during one cycle in each arm. The total number of switching instances per phase with the fundamental frequency f_1 and modulation index m can be approximated as

$$N_{\text{SW}} \approx \sum_{k=(1-m)N/2+1}^{(1+m)N/2} 4f_1 (2k-1). \quad (18)$$

The system switching loss follows

$$P_{\text{SW}} = N_{\text{phase}} N_{\text{SW}} \left(\frac{1}{2} v_{\text{SM}} i_{\text{SM}} (t_{\text{on}} + t_{\text{off}}) \right), \quad (19)$$

where N_{phase} is the total number of phases in the system, v_{SM} is module voltage, and i_{SM} is module current. v_{SM} and

i_{SM} should be recalculated at each switching step. However, the loss calculation procedure can be simplified by using an average model. The average arm current for half of the arm current cycle can be calculated as

$$i_{\text{SM}} = \frac{I_{\text{ph}}}{2N} \left(\sum_{k=1}^N \text{abs} \left(\frac{m}{2} \cos(\varphi) \pm \sin \left(\frac{\pi}{2} k\omega - \varphi \right) \right) \right). \quad (20)$$

The average current is also a good first approximation for the average switching current. Among different NLM methods, PSANLM has lower switching loss because of the lower v_{SM} and better THD.

C. Total Harmonic Distortion

As the literature confirms, voltage THD analysis of MMC and MMSPC coincide [55]. Dahidah and Agelidis calculate the amplitude of the fundamental frequency of the output voltage for different voltage levels and switching events [56]. Among various NLM techniques, PSANLM achieves the lowest THD value. Hence this paper chooses PSANLM for further discussion. The amplitude of the fundamental frequency of PSANLM method is

$$A_1 = \frac{4V_d}{\pi} \sum_{i=1}^{2N} \cos(\alpha_i), \quad (21)$$

where α_i is the switching angle with $0 < \alpha_1 < \dots < \alpha_{2N} < \pi/2$. Considering the calculated amplitudes and output voltage, the THD follows

$$\text{THD} = \frac{\sqrt{\frac{2}{\pi} \sum_{i=0}^{N_\alpha} \left(\int_{\alpha_i}^{\alpha_{i+1}} (V_{i,d} - A_1 \cos(\varphi)) d\varphi \right)^2}}{A_1}, \quad (22)$$

where N_α is $2N$ for PSANLM and $\alpha_0 = 0$. As can be seen, the proposed scheduler has no effect on the output voltage THD value.

V. SIMULATION AND EXPERIMENTAL RESULTS

This section evaluates the performance of the proposed system and compares it with other popular techniques. MATLAB Simulink serves to simulate a system with 40 modules. Furthermore, we built a scaled-down system with eight modules in the lab for experimental evaluation. In both simulation and experiments, the proposed scheduler combined with PSANLM is evaluated and compared to phase-shifted carrier (PSC) modulation as an alternative that includes scheduling. Furthermore, we compare the performance of the proposed scheduler to a conventional cell-sorting scheduler (which highly relies on measurement of module voltages) in both MMSPC and MMC topologies [57] as well as a fixed-switching-pattern scheduler in MMSPC [58], [59].

The implemented cell-sorting algorithm is based on the literature [60]. For MMSPC, we replace each bypass with a parallel connection. The fixed-switching-pattern scheduler inserts the modules into the arm based on their index and without any specific scheduling. The power loss and also the THD output of the PSC heavily rely on the frequency of the carriers: higher carrier frequencies lead to higher switching loss and

TABLE I
SYSTEM PARAMETERS

Parameters	Simulations	Experiments
Rated Power (per arm)	36 kVA	1.25 kVA
dc link Voltage	1200 V	200 V
Number of modules per arm	20	4
modules Capacitance	20 mF	5 mF
Capacitor Resistance	20 mΩ	20 mΩ
Decoupling Inductor	5 μH	7 μH
Decoupling Inductor Resistance	100 μΩ	150 μΩ
Arm Inductor	0.9 mH	1.5 mH
Inductor Resistance	2 mΩ	20 mΩ
Switch Model	IGBT	IPT015N10N5
R_{CE}	1.5 mΩ	1.5 mΩ
V_{CE}	1.5 V	1.5 V
Implementation/Controller	MATLAB	sbRIO9627

lower voltage THD. A fair comparison suggests selecting the minimum carrier frequency that results in an acceptable THD output. The following provides a brief analysis of the THD output of the PSC.

The amplitude of the fundamental frequency voltage using PSC-PWM is

$$A_1 = \frac{8V_d}{\pi} \sum_{i=1}^{(f_{sw}N/2f_1)} (-1)^k \cos(\alpha_i), \quad (23)$$

where $0 < \alpha_1 < \alpha_2 < \dots < \frac{\pi}{2}$ and k in positive step condition is 1, otherwise 0.

Comparing (23) with the THD of the PSANLM shows that for a comparable THD the switching rate in PSC-PWM should be at least four times higher than the fundamental frequency. Systems with a large number of modules require much more switching for a PSC-PWM to obtain similar THD values, which consequently leads to higher switching losses. In systems with lower numbers of modules, where higher switching frequencies are possible, i.e., systems with lower power ratings, PSC-PWM can achieve THD values that are not possible for NLM. Here, the carrier frequency of $11f_1$ for experiments and $4f_1$ for simulations is selected. Table I provides the detailed parameters of the system.

The PSC modulation method uses N carriers with $2\pi/N$ phase difference for each arm with N submodules. This method's performance significantly depends on initial phase difference between the voltage reference and the carriers. Therefore, this comparison uses the optimal carrier distribution [43], which improves the balancing performance and efficiency of the system. The optimal carrier distribution for twenty modules per arm follows

$$\theta_{opt} = [10 \ 19 \ 8 \ 17 \ 6 \ 15 \ 4 \ 13 \ 2 \ 11 \ 0 \ 9 \ 18 \ 7 \ 16 \ 5 \ 14 \ 3 \ 12 \ 1] \times \frac{2\pi}{20} + \theta_{init}, \quad (24)$$

where $\theta_{init} = 2\pi/60$ is the phase difference between the voltage reference and the first carrier. Fig. 6(a) shows the simulation results for output voltages of the five modulation methods. As expected, the output voltage of the proposed method is more sinusoidal. Fig. 6(b) shows THDs of the output voltages, which confirms proper performance of the proposed method. THD of the NLM-based techniques are relatively

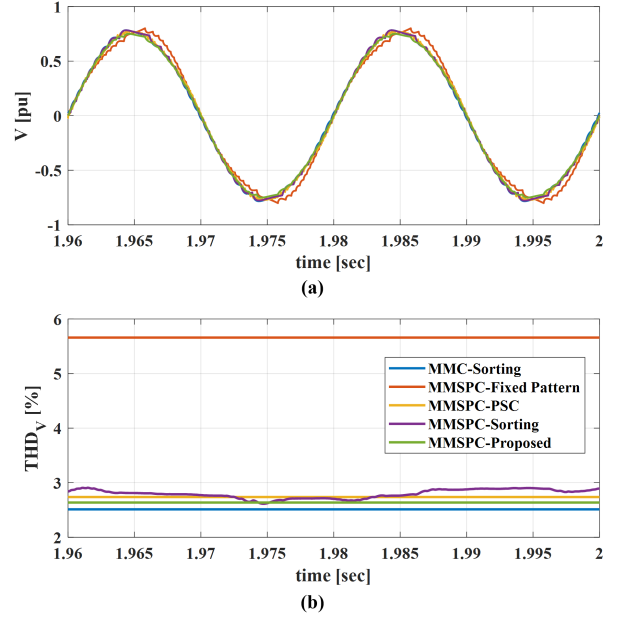


Fig. 6. (a) Waveforms of output voltage of five different modulation methods. (b) Sliding window THD of the waveforms.

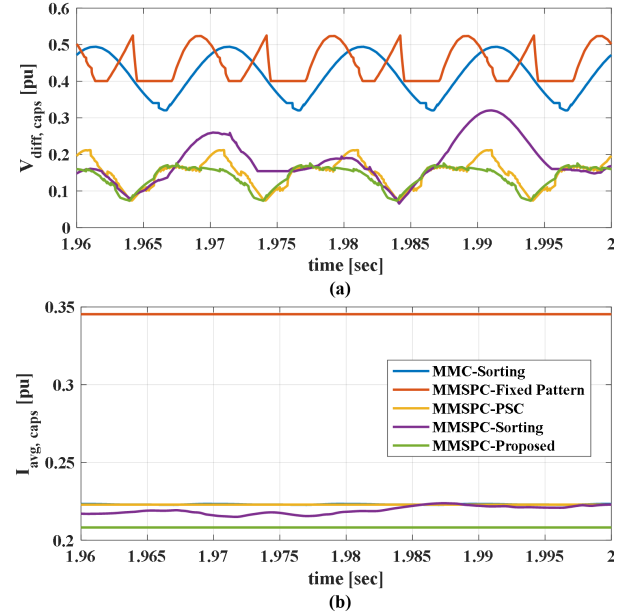


Fig. 7. (a) Voltage differences between modules in each method. (b) Average capacitors current.

similar, with the proposed method providing the best THD for MMSPC topology and the fixed-pattern scheduling the worst. This is mainly due to the effect of the scheduler on the balancing.

Fig. 7 investigates the capacitors voltage balancing performance by comparing the voltage difference between maximum and minimum values for each method. The proposed method has the best performance in capacitor voltages balancing, whereas the fixed-switching-pattern scheduler performs poorest.

The main reason why the proposed scheduler outperforms

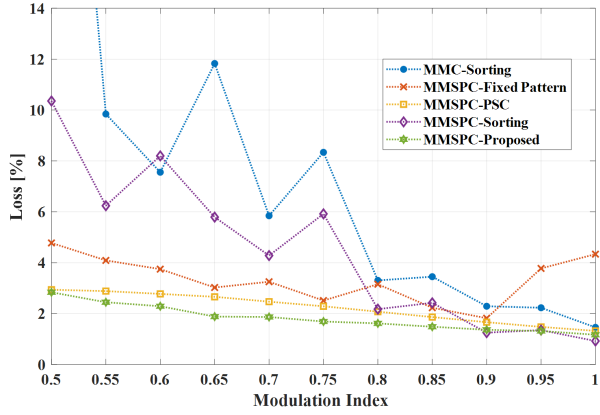


Fig. 8. Comparison of power loss for different methods with modulation index between 0.5 and 1 when capacitor voltages are balanced and load is resistive ($PF=1$).

cell-sorting is lower accumulated voltage imbalance. Furthermore, as shown in Fig. 7, the average capacitor current in the proposed method is lower compared to the other methods, which in turn leads to higher efficiency and the option to use smaller capacitors. The capacitor current is affected by the phase current ($i_{ph} \uparrow \Rightarrow i_{sm} \uparrow$), modulation index ($m \uparrow \Rightarrow i_{sm} \uparrow$), power factor ($PF \uparrow \Rightarrow i_{sm} \uparrow$), and balancing operation ($i_{balancing} \downarrow \Rightarrow i_{sm} \downarrow$). While it is not possible to control the three factors through scheduling, a suitable scheduler can reduce the balancing requirement and hence the average capacitor current. Capacitors are among the bulkiest and most expensive components in the system. Any reduction of their size is a significant advantage worth further analysis. However, since it is not the main focus of this paper, we do not provide further discussion of the capacitor ripple.

Fig. 8 compares the power loss for different modulation indices. It is assumed that the capacitors have the same voltage with the modulation index ranging between 0.5 and 1. Increasing the modulation index reduces the power loss in all methods except the fixed pattern. Power losses of the fixed-switching-pattern scheduler for modulation indices below 0.8 are high, which shows the importance of minimizing the conduction loss. The power loss could be decomposed into conduction and switching loss, which are also compared in Fig. 10 and Fig. 11, respectively.

The proposed method has the lowest power loss compared to the others, including PSC. While the proposed scheduler slightly increases the switching losses, those of NLM are negligible compared to the conduction losses as verified by Fig. 10 and Fig. 11. The analysis of Section IV yields $I_{arm}^{rms} = 49.54$ A and the absolute average arm current $I_{arm}^{avg} = 36.5$ A. Furthermore, the switching and conduction losses are 0.0093 % and 1.59 %. Compared to Fig. 10 and 11, the estimation errors are 0.0004 % and 0.03 %. These results clarify the high efficiency of the proposed method.

All the scheduling methods are simulated with RL load ($PF \approx 0.87$), and Fig. 12 depicts the power losses with respect to modulation index. With RL load, the proposed scheduler achieves the best performance and reduces the average losses by more than 20 %. We further evaluated the power loss in

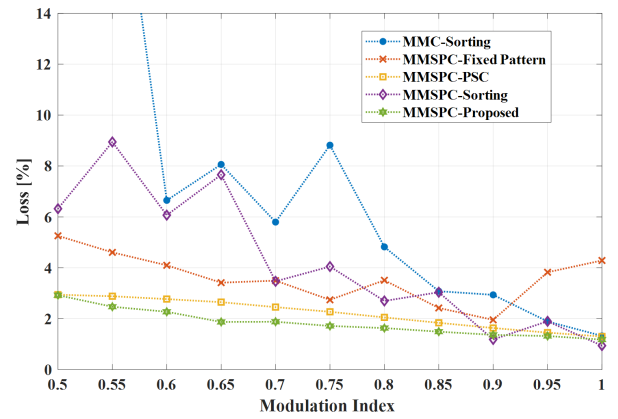


Fig. 9. Comparison of power loss for different methods with modulation index between 0.5 and 1 when capacitor voltages are not balanced and load is resistive ($PF=1$).

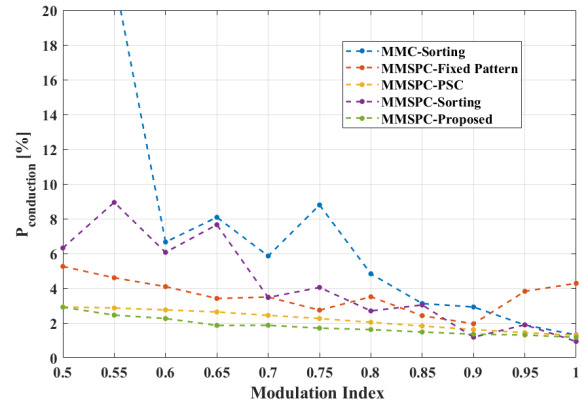


Fig. 10. Comparison of conduction power loss for different methods with modulation index between 0.5 and 1 when capacitor voltages are balanced and load is resistive ($PF=1$).

case of mismatched capacitors in the modules. As shown in Fig. 9, the results are almost the same.

Fig. 13 shows the setup for experimental evaluation. We implemented the modulation and scheduling algorithms on an FPGA development board. There are four modules in each

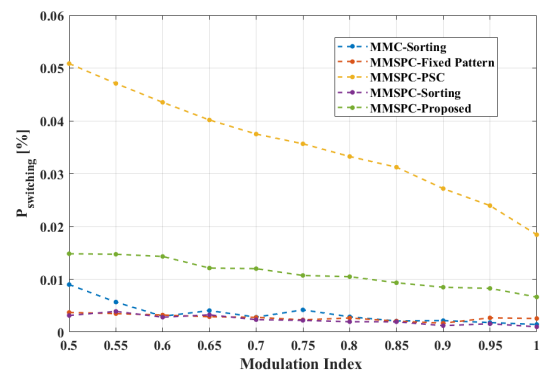


Fig. 11. Comparison of switching power loss for different methods with modulation index between 0.5 and 1 when capacitor voltages are balanced and load is resistive ($PF=1$).

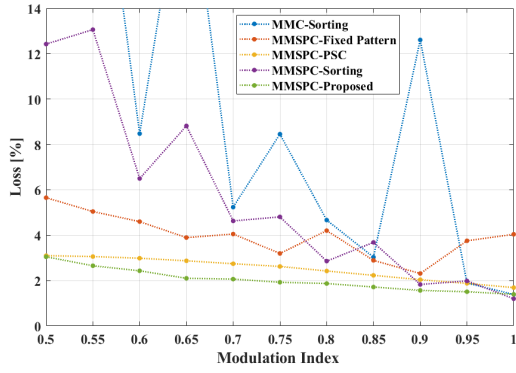


Fig. 12. Comparison of power loss for different methods with modulation index between 0.5 and 1 when capacitor voltages are balanced and load is inductive ($PF \approx 0.87$).

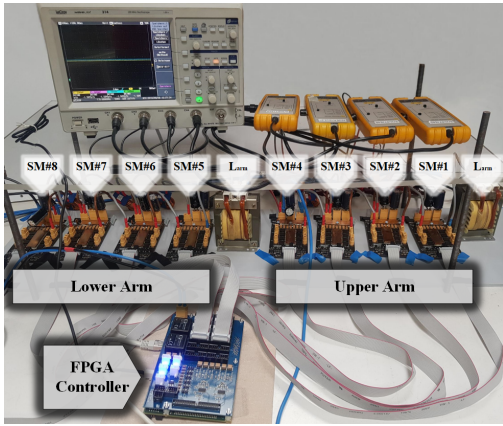
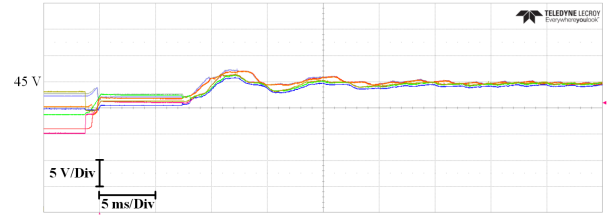


Fig. 13. Laboratory setup for experimental evaluation.

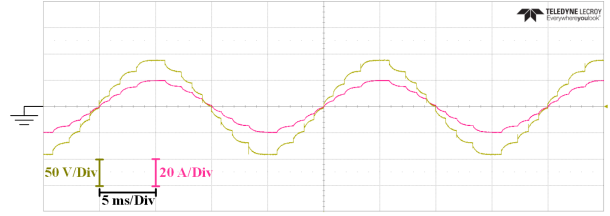
arm and a filter between every two modules (see Table I for values). The output voltage frequency is tuned to 50 Hz, and the load of the system is a 5Ω resistor; a 200 V source supplies the dc link voltage and modulation index is set as 95 %.

Fig. 14 illustrates the measurements for PSANLM with the proposed scheduler with resistive load. Fig. 14(a) confirms the balancing capability of the MMSPC topology and Fig. 14(b) shows the result of PSANLM modulation. In general, the proposed scheduler's effects on the output voltage waveform are negligible and all the scheduler methods with PSANLM will result in mostly similar output shapes. However, the efficiencies vary significantly. It should be mentioned that the THD of the experimental output voltage and ripple of module voltages are expectedly higher than the simulation due to the lower number of modules in the experimental setup. Additionally, lower numbers increase the stress on the inductor and lead to higher voltage ripple.

Fig. 15 illustrates experimental results of the proposed method with highly inductive load. The lower power factor reduces the discharge of the capacitors when the modules are in series and leads to more defined step shapes in the output voltage of the system. Thus, the proposed method is not power-factor dependent. For comparison, experimental results of the PSC method are captured and shown in Fig. 16 and 17 for

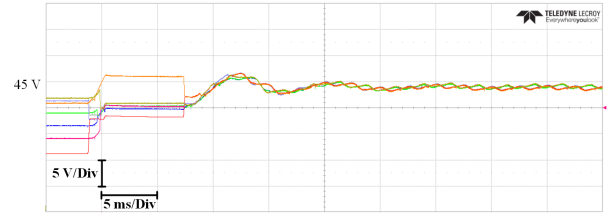


(a)

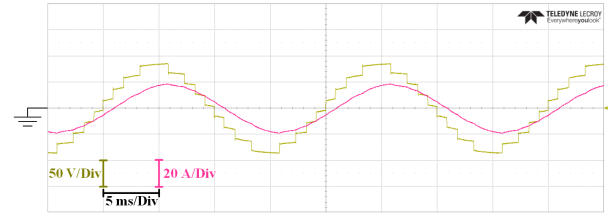


(b)

Fig. 14. Experimental results for the proposed method with resistive load ($PF = 1$), a) different module voltages, b) AC output voltage and current.

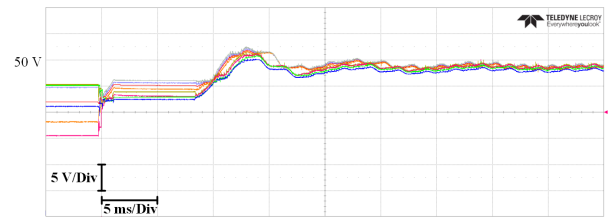


(a)

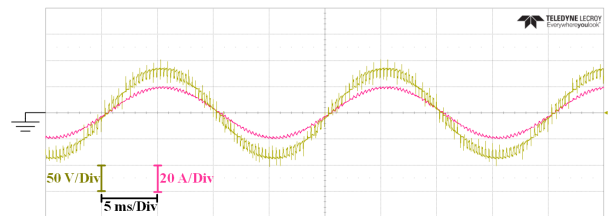


(b)

Fig. 15. Experimental results for the proposed method with inductive load ($PF \approx 0.87$), a) different module voltages, b) AC output voltage and current.



(a)



(b)

Fig. 16. Experimental results for PSC method with resistive load ($PF = 1$), a) different module voltages, b) AC output voltage and current.

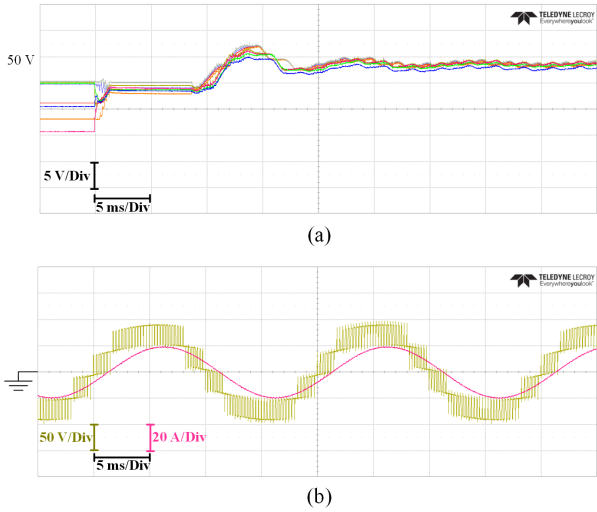


Fig. 17. Experimental results for PSC method with inductive load (PF \approx 0.87), a) different module voltages, b) AC output voltage and current.

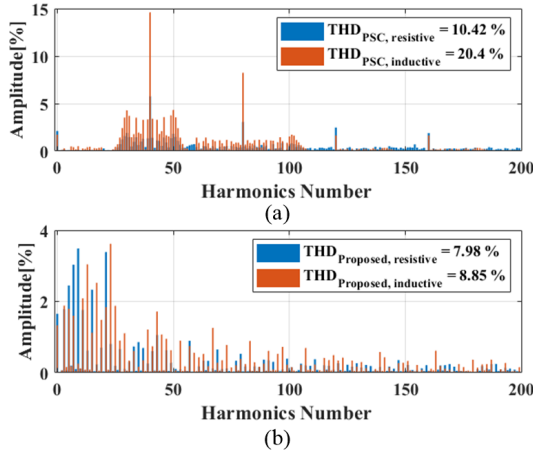


Fig. 18. Graph of the harmonic contents for PSC and proposed modulations, (a) PSC method, (b) proposed method.

PF=1 and PF \approx 0.87, respectively. Here as in the simulation, the output voltage of the proposed method is clearly more sinusoidal. In Fig. 18, the THD value of the output voltages for experimental results have been analyzed. As expected, based on the measurements, the THD of the PSANLM is significantly better than the PSC method. Although, the main harmonics content of PSC modulation are in higher harmonics which simplify filtering, it should be mentioned that the nearest-level modulation is most suitable for systems with higher number of modules and as the simulation results verify, the resultant THDs can be significantly lower.

VI. CONCLUSION

This paper proposes a new scheduling algorithm to minimize the conduction loss of MMCs with additional parallel connectivity between modules. It further discusses the combination of the proposed method with low-frequency switching. However, the proposed method is compatible with any high-level control. Regardless of the combination of the proposed

algorithm with various modulators, the algorithm achieves the best configuration with minimum conduction loss. The optimal configuration improves the capacitor voltage balancing and reduces the balancing current. In addition, the algorithm is easily scalable to large systems.

Methods with high computational burden are not proper for online and/or cost-effective implementation. These methods require powerful processors and large memory. Some methods try to resolve this issue by limiting the number of feasible solutions, but the computational burden still requires powerful and expensive controllers [61]–[64]. Online implementation of the proposed method is efficient. Importantly, extending it to larger system does not increase the computational load.

The method is evaluated in simulations and experiments; the results confirm the effectiveness and simplicity of the proposed method in terms of voltage balancing, THD, and efficiency. The numerical comparisons show that the power loss is reduced 18–55% in either balanced or imbalance modes compared to other scheduling techniques. Furthermore, averaged capacitor current is improved 7.5% compared to PSC.

REFERENCES

- [1] M. Sandhu and T. Thakur, “Multilevel inverters: Literature survey—topologies, control techniques & applications of renewable energy sources-grid integration,” *Int. Journal of Engineering Research and Applications*, vol. 4, no. 3, pp. 644–652, 2014.
- [2] A. Kaymanesh, A. Chandra, and K. Al-Haddad, “Model predictive control of mpuc7-based statcom using autotuned weighting factors,” *IEEE Transactions on Industrial Electronics*, pp. 1–1, 2021.
- [3] M. Guan and Z. Xu, “Modeling and control of a modular multilevel converter-based hvdc system under unbalanced grid conditions,” *IEEE transactions on power electronics*, vol. 27, no. 12, pp. 4858–4867, 2012.
- [4] J. Qin and M. Saedifard, “Predictive control of a modular multilevel converter for a back-to-back hvdc system,” *IEEE Transactions on Power Delivery*, vol. 27, no. 3, pp. 1538–1547, 2012.
- [5] B. P. McGrath, C. A. Teixeira, and D. G. Holmes, “Optimized phase disposition (pd) modulation of a modular multilevel converter,” *IEEE Transactions on Industry Applications*, vol. 53, no. 5, pp. 4624–4633, 2017.
- [6] L. Zhang, Y. Tang, S. Yang, and F. Gao, “Decoupled power control for a modular-multilevel-converter-based hybrid ac–dc grid integrated with hybrid energy storage,” *IEEE Transactions on Industrial Electronics*, vol. 66, no. 4, pp. 2926–2934, 2019.
- [7] N. Thitichaiworakorn, M. Hagiwara, and H. Akagi, “Experimental verification of a modular multilevel cascade inverter based on double-star bridge cells,” *IEEE Transactions on Industry Applications*, vol. 50, no. 1, pp. 509–519, 2013.
- [8] V. Spudić and T. Geyer, “Model predictive control based on optimized pulse patterns for modular multilevel converter statcom,” *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6137–6149, 2019.
- [9] S. Debnath, J. Qin, B. Bahrani, M. Saedifard, and P. Barbosa, “Operation, control, and applications of the modular multilevel converter: A review,” *IEEE transactions on power electronics*, vol. 30, no. 1, pp. 37–53, 2014.
- [10] F. Deng, Y. Tian, R. Zhu, and Z. Chen, “Fault-tolerant approach for modular multilevel converters under submodule faults,” *IEEE Transactions on Industrial Electronics*, vol. 63, no. 11, pp. 7253–7263, 2016.
- [11] J. Wang, X. Han, H. Ma, and Z. Bai, “Analysis and injection control of circulating current for modular multilevel converters,” *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2280–2290, 2018.
- [12] Y. Meng, Y. Zou, H. Wang, Y. Kong, Z. Du, and X. Wang, “Novel submodule topology with large current operation and dc-fault blocking capability for mmc-hvdc,” *IEEE Transactions on Power Delivery*, vol. 36, no. 3, pp. 1542–1551, 2021.

- [13] Y. Jin, Q. Xiao, C. Dong, H. Jia, Y. Mu, B. Xie, Y. Ji, S. K. Chaudhary, and R. Teodorescu, "A novel submodule voltage balancing scheme for modular multilevel cascade converter—double-star chopper-cells (mmcc-dscc) based statcom," *Ieee Access*, vol. 7, pp. 83 058–83 073, 2019.
- [14] C. Gao and J. Lv, "A new parallel-connected diode-clamped modular multilevel converter with voltage self-balancing," *IEEE Transactions on Power Delivery*, vol. 32, no. 3, pp. 1616–1625, 2017.
- [15] A. A. Taffese, E. de Jong, S. D'Arco, and E. Tedeschi, "Online parameter adjustment method for arm voltage estimation of the modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 12 491–12 503, 2019.
- [16] Y. Deng, Y. Wang, K. H. Teo, M. Saedifard, and R. G. Harley, "Optimized control of the modular multilevel converter based on space vector modulation," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5697–5711, 2017.
- [17] J. Fang, H. Deng, N. Tashakor, F. Blaabjerg, and S. M. Goetz, "State-space modeling and control of grid-tied power converters with capacitor/battery energy storage and grid-supportive services," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2021.
- [18] G. Chen, H. Peng, R. Zeng, Y. Hu, and K. Ni, "A fundamental frequency sorting algorithm for capacitor voltage balance of modular multilevel converter with low-frequency carrier phase shift modulation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1595–1604, 2017.
- [19] K. Wang, Y. Deng, H. Peng, G. Chen, G. Li, and X. He, "An improved cps-pwm scheme-based voltage balancing strategy for mmc with fundamental frequency sorting algorithm," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2387–2397, 2018.
- [20] J. Fang, F. Blaabjerg, S. Liu, and S. Goetz, "A review of multilevel converters with parallel connectivity," *IEEE Transactions on Power Electronics*, pp. 1–1, 2021.
- [21] Z. Li, R. Lizana F., Z. Yu, S. Sha, A. V. Peterchev, and S. M. Goetz, "A modular multilevel series/parallel converter for a wide frequency range operation," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9854–9865, 2019.
- [22] J. Fang, S. Yang, H. Wang, N. Tashakor, and S. M. Goetz, "Reduction of mmc capacitances through parallelization of symmetrical half-bridge submodules," *IEEE Transactions on Power Electronics*, vol. 36, no. 8, pp. 8907–8918, 2021.
- [23] N. Tashakor, Z. Li, and S. M. Goetz, "A generic scheduling algorithm for low-frequency switching in modular multilevel converters with parallel functionality," *IEEE Transactions on Power Electronics*, vol. 36, no. 3, pp. 2852–2863, 2021.
- [24] S. M. Goetz, A. V. Peterchev, and T. Weyh, "Modular multilevel converter with series and parallel module connectivity: Topology and control," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 203–215, 2015.
- [25] M. Uno, K. Yashiro, and K. Hasegawa, "Modularized equalization architecture with voltage multiplier-based cell equalizer and switchless switched capacitor converter-based module equalizer for series-connected electric double-layer capacitors," *IEEE transactions on power electronics*, vol. 34, no. 7, pp. 6356–6368, 2018.
- [26] Z. Li, R. Lizana, A. V. Peterchev, and S. M. Goetz, "Distributed balancing control for modular multilevel series/parallel converter with capability of sensorless operation," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 1787–1793.
- [27] Z. Li, J. K. Motwani, Z. Zeng, S. M. Lukic, A. V. Peterchev, and S. M. Goetz, "A reduced series/parallel module for cascade multilevel static compensators supporting sensorless balancing," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 1, pp. 15–24, 2021.
- [28] Q. Tu, Z. Xu, and L. Xu, "Reduced switching-frequency modulation and circulating current suppression for modular multilevel converters," *IEEE transactions on power delivery*, vol. 26, no. 3, pp. 2009–2017, 2011.
- [29] A. Hassanpoor, S. Norrga, H.-P. Nee, and L. Ångquist, "Evaluation of different carrier-based pwm methods for modular multilevel converters for hvdc application," in *IECON 2012-38th Annual Conference on IEEE Industrial Electronics Society*. IEEE, 2012, pp. 388–393.
- [30] D. Siemaszko, A. Antonopoulos, K. Ilves, M. Vasiladiotis, L. Ångquist, and H.-P. Nee, "Evaluation of control and modulation methods for modular multilevel converters," in *The 2010 International Power Electronics Conference-ECCE ASIA*-. IEEE, 2010, pp. 746–753.
- [31] F. Deng and Z. Chen, "A control method for voltage balancing in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 66–76, 2013.
- [32] M. Quraan, T. Yeo, and P. Tricoli, "Design and control of modular multilevel converters for battery electric vehicles," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 507–517, 2016.
- [33] P. Hu, R. Teodorescu, S. Wang, S. Li, and J. M. Guerrero, "A currentless sorting and selection-based capacitor-voltage-balancing method for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1022–1025, 2018.
- [34] D. Samajdar, T. Bhattacharya, and S. Dey, "A reduced switching frequency sorting algorithm for modular multilevel converter with circulating current suppression feature," *IEEE Transactions on Power Electronics*, vol. 34, no. 11, pp. 10 480–10 491, 2019.
- [35] A. António-Ferreira, C. Collados-Rodríguez, and O. Gomis-Bellmunt, "Modulation techniques applied to medium voltage modular multilevel converters for renewable energy integration: A review," *Electric Power Systems Research*, vol. 155, pp. 21–39, 2018.
- [36] J. Huang, B. Yang, F. Guo, Z. Wang, X. Tong, A. Zhang, and J. Xiao, "Priority sorting approach for modular multilevel converter based on simplified model predictive control," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4819–4830, 2017.
- [37] K. Ilves, F. Taffner, S. Norrga, A. Antonopoulos, L. Harnefors, and H.-P. Nee, "A submodule implementation for parallel connection of capacitors in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 7, pp. 3518–3527, 2014.
- [38] S. M. Goetz, Z. Li, A. V. Peterchev, X. Liang, C. Zhang, and S. M. Lukic, "Sensorless scheduling of the modular multilevel series-parallel converter: enabling a flexible, efficient, modular battery," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*. IEEE, 2016, pp. 2349–2354.
- [39] N. Tashakor, B. Arabsalmanabadi, L. O. Cervera, E. Hosseini, K. Al-Haddad, and S. Goetz, "A simplified analysis of equivalent resistance in modular multilevel converters with parallel functionality," in *IECON 2020 The 46th Annual Conference of the IEEE Industrial Electronics Society*, 2020, pp. 4158–4163.
- [40] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 1, pp. 77–88, 2014.
- [41] O. Theliander, A. Kersten, M. Kuder, W. Han, E. A. Grunditz, and T. Thiringer, "Battery modeling and parameter extraction for drive cycle loss evaluation of a modular battery system for vehicles based on a cascaded h-bridge multilevel inverter," *IEEE Transactions on Industry Applications*, vol. 56, no. 6, pp. 6968–6977, 2020.
- [42] K. Ilves, L. Bessegato, L. Harnefors, S. Norrga, and H.-P. Nee, "Semi-full-bridge submodule for modular multilevel converters," in *2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia)*. IEEE, 2015, pp. 1067–1074.
- [43] Z. Li, R. Lizana, S. Sha, Z. Yu, A. V. Peterchev, and S. M. Goetz, "Module implementation and modulation strategy for sensorless balancing in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8405–8416, 2018.
- [44] S. M. Goetz, Z. Li, X. Liang, C. Zhang, S. M. Lukic, and A. V. Peterchev, "Control of modular multilevel converter with parallel connectivity—application to battery systems," *IEEE Transactions on Power Electronics*, vol. 32, no. 11, pp. 8381–8392, 2016.
- [45] S. K. Patro and A. Shukla, "Control and derived topologies of parallel hybrid converter," *IEEE Transactions on Industry Applications*, vol. 57, no. 1, pp. 598–613, 2021.
- [46] B. Arabsalmanabadi, H. Arab, V. H. G. Amador, S. Dufour, and K. Al-Haddad, "A three-dimensional discontinuous galerkin time-domain finite element method for electromagnetic modeling of wireless power transfer coils," *IEEE Open Journal of the Industrial Electronics Society*, vol. 2, pp. 360–371, 2021.
- [47] P. Hu and D. Jiang, "A level-increased nearest level modulation method for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 1836–1842, 2014.
- [48] N. Tashakor, M. Kilicatas, J. Fang, and S. Goetz, "Switch-clamped modular multilevel converters with sensorless voltage balancing control," *IEEE Transactions on Industrial Electronics*, 2020.
- [49] M. Merlin, T. Green, P. Mitcheson, F. Moreno, K. Dyke, and D. Trainer, "Cell capacitor sizing in modular multilevel converters and hybrid topologies," in *2014 16th European Conference on Power Electronics and Applications*. IEEE, 2014, pp. 1–10.
- [50] A. Kavousi, B. Vahidi, R. Salehi, M. K. Bakhshizadeh, N. Farokhnia, and S. H. Fathi, "Application of the bee algorithm for selective harmonic elimination strategy in multilevel inverters," *IEEE Transactions on power electronics*, vol. 27, no. 4, pp. 1689–1696, 2011.
- [51] N. Tashakor, M. Kilicatas, E. Bagheri, and S. Goetz, "Modular multilevel converter with sensorless diode-clamped balancing through level-

- adjusted phase-shifted modulation," *IEEE Transactions on Power Electronics*, pp. 1–1, 2020.
- [52] X. Hu, Y. Zhu, J. Zhang, F. Deng, and Z. Chen, "Unipolar double-star submodule for modular multilevel converter with dc fault blocking capability," *IEEE Access*, vol. 7, pp. 136 094–136 105, 2019.
- [53] G. Lu, C. Gao, and X. Li, "Voltage self-balance method for series connected igbts by using clamping diodes," in *IECON 2017-43rd Annual Conference of the IEEE Industrial Electronics Society*. IEEE, 2017, pp. 5000–5005.
- [54] M. Quraan, P. Tricoli, S. D'Arco, and L. Piegari, "Efficiency assessment of modular multilevel converters for battery electric vehicles," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 2041–2051, 2016.
- [55] M. Sharifzadeh, H. Vahedi, R. Portillo, L. G. Franquelo, and K. Al-Haddad, "Selective harmonic mitigation based self-elimination of triplen harmonics for single-phase five-level inverters," *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 86–96, 2018.
- [56] M. S. Dahidah and V. G. Agelidis, "Selective harmonic elimination pwm control for cascaded multilevel voltage source converters: A generalized formula," *IEEE Transactions on power electronics*, vol. 23, no. 4, pp. 1620–1630, 2008.
- [57] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings*, vol. 3. IEEE, 2003, pp. 6–pp.
- [58] S. M. Goetz, C. Wang, Z. Li, D. L. Murphy, and A. V. Peterchev, "Concept of a distributed photovoltaic multilevel inverter with cascaded double h-bridge topology," *International Journal of Electrical Power & Energy Systems*, vol. 110, pp. 667–678, 2019.
- [59] C. Wang, A. V. Peterchev, and S. M. Goetz, "Online switch open-circuit fault diagnosis using reconfigurable scheduler for modular multilevel converter with parallel connectivity," in *2019 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)*. IEEE, 2019, pp. P–1.
- [60] Y. Wang, C. Hu, R. Ding, L. Xu, C. Fu, and E. Yang, "A nearest level pwm method for the mmc in dc distribution grids," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9209–9218, 2018.
- [61] Y. Liu and F. Z. Peng, "A modular multilevel converter with self-voltage balancing part i: Mathematical proof," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1117–1125, 2019.
- [62] —, "A modular multilevel converter with self-voltage balancing part ii: Y-matrix modulation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 2, pp. 1126–1133, 2019.
- [63] A. Ghazanfari and Y. A.-R. I. Mohamed, "A hierarchical permutation cyclic coding strategy for sensorless capacitor voltage balancing in modular multilevel converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 2, pp. 576–588, 2015.
- [64] Z. Li, R. Lizana, A. V. Peterchev, and S. M. Goetz, "Predictive control of modular multilevel series/parallel converter for battery systems," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 5685–5691.