Switch-Clamped Modular Multilevel Converters with Sensorless Voltage Balancing Control

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***Abstract*—Modular multilevel converters (MMCs) are an established topology for highest voltage and power levels. For lower levels, MMC finds a wide range of applications in generation, energy storage, and electric motor drive. However, the large quantity of expensive voltage sensors as well as high data-processing requirements for module voltage balancing remain as an obstacle. Additionally, stark cost reductions of power electronic semiconductors have reduced their share in the total cost and rendered initially uneconomical module topologies appealing in low- and medium voltages. This paper proposes an MMC topology with an active clamping path that balances the voltage of the modules in an arm. The proposed structure can achieve sensorless voltage balancing with minimum control effort. The sensorless operation has the added benefit of reducing the communication as well as computation demand between the modules and the central controller. As compared with state-of-the-art voltage balancing schemes, the proposed solution achieves balanced system operation with less power loss, fewer components, and without any measurement. The presented analysis as well as simulation and experimental results verify the benefits of the proposed topology. The results demonstrate that even in the face of a severe imbalance, all the module voltages are maintained within tight boundaries.**

***Index Terms*—Modular multilevel converter (MMC), cascaded H bridge, active clamp circuit, sensorless operation, topology, snubber design.**

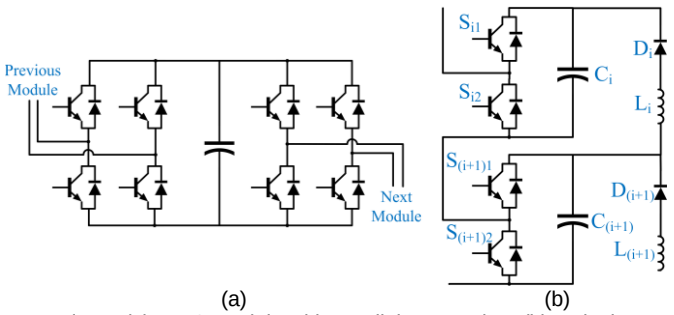
I. Introduction

Modular multilevel converters (MMCs) are increasingly deployed in renewable generation, energy storage, and electric motor drive [1]. Modularity, scalability, high power quality, reliability, and flexibility are main advantages that make MMCs stand out among two-level and other multilevel converters [2]. However, there are a few challenges that hinder the further development and deployment of MMCs, particularly in small and medium systems, where the hardware for fast monitoring and control is too costly [3]. One major challenge refers to the imbalance of module voltages due to parameter tolerances, parasitics, or unsuitable module voltage control, leading to malfunction of MMCs [4, 5].

A conventional solution to the balancing challenge is cell sorting, where the modules with the lowest or highest voltages are firstly connected to be charged or discharged by the arm current to achieve a more balanced state [6-8]. The relevant algorithms are called module schedulers or balancers [9, 10]. Cell sorting algorithms demand high computational power in large systems and researchers have tried to reduce the computational demand. For example, Deng et al. proposes a decentralized balancing approach, where the current of each module is controlled independently [11], while Wang et al. present a sorting algorithm with lower frequency in combination with a phase-shifted carrier modulation [12]. Although feasible, closed-loop balancing algorithms highly rely on the accurate and fast measurement of module voltages [13]. However, the implementation of fast, accurate, and galvanically isolated voltage sensors greatly increases the cost of MMCs. This extra cost and complexity is unfavorable in high-voltage applications with hundreds of modules and renders the MMC practically uncompetitive in low- and medium-voltage applications, where the power transistors are typically wired right to a control system [14].

Many software-based solutions have been proposed to remove/reduce voltage sensors. Some balance module voltages through complicated fixed switching patterns [15-18], whereas others focus on the estimation of module voltages and reduce [19] or entirely eliminate cost of voltage measurement to facilitate expansion of MMCs to cost-competitive applications [20, 21]. In addition to complexity, methods based on such fixed switching sequences attempt to evenly distribute loads to identical modules, but they cannot ensure balanced operation within a tight boundary in case of module mismatches. In contrast, voltage estimation methods heavily rely on system models. Although accurate models can allow accurate estimation, practical models for voltage estimation are susceptible to component tolerances and/or system parameter changes (e.g., capacitance variations or increased turn-on resistances of switches due to aging) [21]. Additionally, voltage estimation techniques rely on accurate measurement of the output parameters such as arm current or output voltage. Because of the susceptibility to accumulative measurement errors, even small offsets of the measurement can lead to divergence in the long run. Complexity and limited balancing capability are two other drawbacks of voltage-estimation methods.

Hardware-based solutions can be a more stable alternative without above-given limitations. Although topology modifications can eliminate many voltage sensors and their corresponding cost, the additional cost of power semiconductors can be detrimental in ultra-high-voltage applications. However, the share of control and monitoring electronics in the total cost is higher at lower voltages.



(a) (b)

Fig. 1. (a) MMC module with parallel connection; (b) typical diode-clamped circuit

Thus, ensuring balancing from a hardware and topology side can lead to more noticeable cost savings [1].

Furthermore, many low- to medium-voltage applications need a strict (functional) safety concept, which can require high safety integrity levels (SIL) for the balancing (such as SIL 3 and higher). Consequently, the entire monitoring chain and particularly the communication bus inherit the level, which exacerbates development and verification. A hardware fallback mechanism that enforces balancing can on the other hand ensure the SIL level whereas the balancing system including monitoring and communication hardware, could be developed following regular quality-management procedures only, substantially reducing cost [22, 23].

In addition to cost reduction and lower safety constraints, a combination of topology-based solutions with monitoring can reduce the bandwidth requirements. Particularly in more recent MMCs with hundreds of modules and rapid capacitor-voltage fluctuations due to capacitance reductions, monitoring of all module voltages with sufficient sampling rate requires substantial communication bandwidth and data processing power. Additional hardware balancing can reduce the number of necessary sensors and/or the sampling rate [24, 25].

For self-balancing MMC topologies, the conventional topologies of modules are modified in order to provide balancing with less measurement requirements [26-28]. As an example, voltage mismatches can be canceled through parallelization of double H-bridge modules as shown in Fig. 1(a) [29, 30]. Along this research direction, Xu et al. developed two novel MMC topologies based on half-bridge and full-bridge modules [31]. Sensorless operation, improved efficiency, and increased current rating are major advantages of MMCs with parallel connectivity [32]. However, these advantages are achieved at the expense of more individual semiconductor switches paired with associated drivers and complexity, which can hamper the translation of such novel MMC technologies to high-voltage applications [31].

Diode-clamped topologies—which replace transistors and their drivers with rectifiers—are simpler and more cost-effective, as shown in Fig. 1(b). They achieve balanced operation by adding one extra diode in each module that connects the high-side of the dc links between neighboring modules. Together with the main switches, these additional diodes enable capacitors to be connected in parallel, and hence balanced in certain cases. However, since the diode only allows unipolar power transfer (i.e., from the lower module to the upper one), the voltage imbalance remains if the voltage of the upper capacitor is higher.

To further achieve bidirectional voltage balance, Gao et al. propose an isolated transformer that links the first and the last modules [26]. However, the high-frequency transformer should withstand the complete voltage of the arm. Also, the voltage balance of neighboring modules may involve the participation of all modules, leading to increased power losses. With the topology in Fig. 1(b), Yin et al. [33] and Liu et al. [34] propose to measure the voltage of the top module that has the highest voltage level and utilize a closed-loop controller to achieve voltage balancing during operation. In case of any imbalance, the top module in the arm would have the highest voltage due to diode-clamped circuits. By controlling this module voltage, one can guarantee a state of balanced operation. However, this method inevitably necessitates an additional isolated voltage sensor and an extra feedback loop that can affect ac voltage control.

Another solution uses two strings in parallel in each arm with opposite balancing current directions, and each string shares half the load [27]. However, this solution doubles the number of required components. As a promising alternative, a self-balancing MMC topology with two different balancing paths is proposed in [35], as shown in Fig. 2(a). There, two different balancing paths are added to each module and the main current path is unchanged, whereas in [27] two different current path exist for the main current and the number of modules is doubled. Notably, a typical diode-clamped path allows unipolar energy transfer, e.g., from C_{i+1} to C_i. Furthermore, an additional fully-controlled switch (such as an IGBT) in combination with a diode can enable energy transfer in the reverse direction, and thus ensure sensorless voltage balancing. The small inductors in each path serve to smoothen current spikes caused by module parallelization [35]. Although this solution is remarkably effective and straightforward, the additional components, including two diodes, one active switch, and two inductors in each module, can still increase the cost of this topology.

Combining the two balancing paths in Fig. 2(a) can simplify the system and thereby reduce overall cost. As such, this paper proposes a switch-clamped balancing topology with reduced active and passive components. The proposed topology has the advantages of simplicity, sensorless voltage balancing, and reduced balancing power loss. Fig. 2(b) shows the proposed topology, which can be considered as a combination of the two balancing paths depicted in Fig. 2(a).

Table I provides a general comparison of existing topologies/algorithms with balancing capabilities and the proposed structure. As observed, the main contributions and advantages of the proposed balancing topology include:

- Reduced number of semiconductor devices compared to other self-balancing topologies
- Sensorless operation capability
- No modification of the main control algorithm and no extra control signal required, which allows for utilizing the proposed method with already implemented systems
- Improved balancing efficiency due to reduced number of serial components
- No need for high-voltage transformers and/or extra parallel strings
- Independence from arm and phase controls, which improves the extendability of the system
- Providing a detailed efficiency analysis and derivation of the optimum switching frequency

The remainder of this paper is organized as follows. Section II studies the balancing principle of the topology, discusses power losses, and conducts a general comparison with state-of-the-art topologies. Sections III and IV present simulation and experiment results, respectively. Finally, we conclude the paper in Section V.

II. Operating Principle of the Proposed Topology

This section describes the proposed charge balancing structure and its working principle. Fig. 2 (b) shows the proposed clamping topology. It consists of a conventional half-bridge-based MMC circuit consisting of n modules and (n–1) additional clamping units in each arm, where n is a positive integer. Each clamping unit includes a series connection of one active switch (e.g., an IGBT with a free-wheeling diode) and an inductor.

TABLE I
GENERAL COMPARISON OF SOFTWARE- AND HARDWARE- BASED BALANCING METHODS

	Method	Ref.	Switch	Diode	Inductor	Comments	Advantages	Disadvantages
Software-Based Approaches	**Decentralized balancing of module voltages**	[11]	$2n$	0	0	Controls the current of modules in a decentralized manner	Easier adaptation in larger systems	High number of voltage sensors; high number of processors
	Fixed switching pattern	[18]	$2n$	0	0	The complete switching pattern is stored, and the patterns are selected in a cyclic manner	Guaranteed convergence under normal conditions; no additional sensor	Complicated pattern should be precalculated; sensitive to different self-discharge rates
	CPS-PWM scheme	[12, 36]	$2n$	0	0	Phase shifted carrier is combined with a low-frequency sorting algorithm	Quick convergence; low-frequency sorting needs lower computation	Requires the online monitoring of the SM voltages; sorting can be still demanding on the processor; voltage sensors
	Sorting and selection method	[37]	$2n$	0	0	Utilizes the previous sorting results in combination with the module voltages	Lower computational burden; relatively good balancing capability	Sensitive to parameter variations; sorting is more demanding than the hardware approaches; voltage sensors
	Sorting and selection method	[38]	$2n$	0	0	Calculates the arm current direction using the module voltages variation and then performs cell sorting	No arm current required; lower sampling rate	Voltage sensor; higher computational burden compared to hardware–based approaches
	Adaptive voltage balancing	[39]	$2n$	0	0	Reduces the switching numbers by predicting the voltage variations and implementing cell sorting	Reduced switching occurrences; voltage sensors	Sensitive to parameter variation; higher computational demand compared to normal cell sorting
	Voltage estimation method	[40]	$2n$	0	0	Estimates the module voltages and removes the cost of voltage sensor	Lower voltage sensor	Sensitive to sensor bias; sensetive to parameter variation
Hardware-Based Approaches	**Diode-clamped**	[26]	$2n+4$	$n+3$	0	Achieves bi-directional balancing by a high-voltage transformer connecting bottom and top modules together	Low sensitivity to parameter variations; lower voltage sensors	Multiple power conversion stages can affect the efficiency; extra transformer increases the cost
	Dual string diode-clamped	[27]	$4n$	$2n$	$2n$	Two separate string are connected in parallel to form an arm, where each string has a different balancing direction.	Sharing the power between strings; sensorless operation	High number of components increases the cost
	MMSPC	[28]	$4n-4$	0	$2n-2$	Provides parallel connection for the modules and realize balancing through parallel functionality	Four quadrant operation; Improved efficiency; sensorless operation	Two extra switches and one additional capacitor increases the cost
	Two parallel clamping clusters	[35]	$3n-1$	$2n-2$	$2n-2$	A diode-clamped and a switch-clamped balancing path in parallel	Sensorless operation; simple control	Lower efficiency; medium number of components
	Diode-clamped	[41, 42]	$2n$	n	n	Controls the voltage of the top module to ensure a balanced operation	Fast SM voltage balancing; DC fault ride-through ability	Requires measurement of top module voltage; extra diodes
	Proposed Method		$3n-1$	0	$n-1$	Utilized a simple and efficient control using one bi-directional balancing path	Sensorless operation; Improved efficiency; simple control	Extra switches and inductors

A. *Clamping Principle*

When capacitor C_{i+1} is bypassed (by turning $S_{(i+1)2}$ on), it is possible to connect C_i and C_{i+1} in parallel through switch–diode pair Q_i and hence, balance the two capacitors. Depending on the capacitors' voltages, the two possibilities for the balancing current are highlighted in Figs. 3(a) and (b). As shown, capacitor voltages can be equalized or balanced in both directions. In low-voltage applications, the proposed IGBT–diode set in the clamping circuit can evidently be implemented with a single MOSFET and its body diode. Therefore, in order to achieve sensorless balancing,we proposed to trigger the switch Q_i of the clamping circuit and $S_{(i+1)2}$ simultaneously, as depicted in Fig. 4. The inductor L_i limits the current spikes during the initial moments and further improves the system efficiency. Depending on the current direction, two situations are possible:

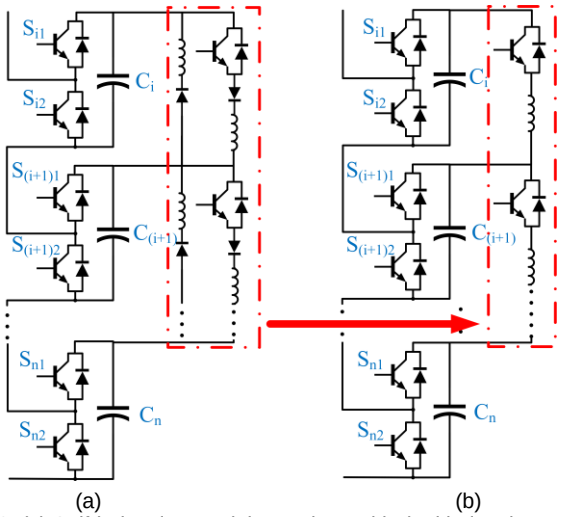


Fig. 2. (a) Self-balancing module topology with dual balancing paths; (b) proposed clamping topology

Situation 1: If the voltage of capacitor C_i is larger than that of capacitor C_{i+1}, i.e., $u_{Ci} > u_{C(i+1)}$, switches $S_{(i+1)2}$ and Q_i can be turned on to let the balancing current flow from C_i to C_{i+1}. This current flow results in the increase of $u_{C(i+1)}$ and the decrease of u_{Ci}, and finally equilibration. The equivalent circuit of the system during

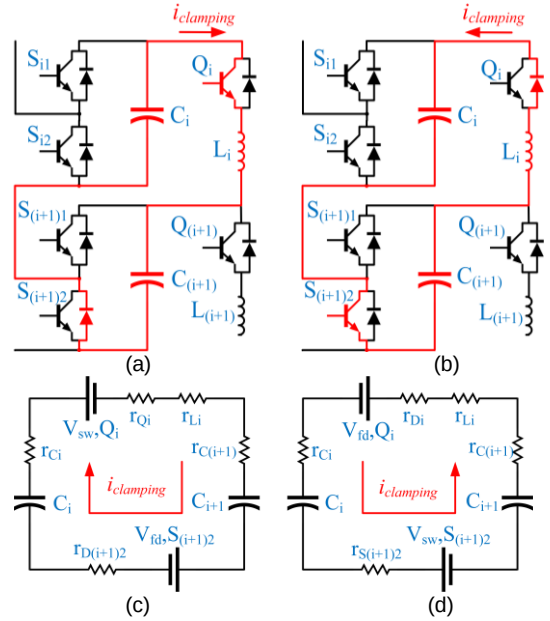


Fig. 3. (a) Clamping path if $u_{Ci} > u_{Ci+1}$; (b) clamping path if $u_{Ci+1} > u_{Ci}$; (c) equivalent circuit for situation 1; (d) equivalent circuit for situation 2

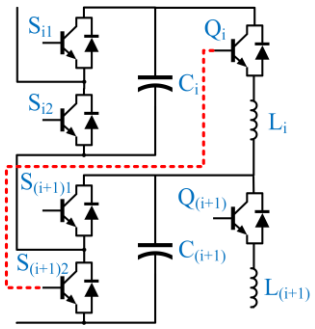


Fig. 4. Gate signal of the switch of clamping circuit.

this situation is shown in Fig. 3(c), where V_{sw} is the IGBT forward voltage drop and V_{fd} is the free-wheeling diode voltage drop. After turning Q_i off, the inductor current goes to zero.

Situation 2: If the voltage of the C_{i+1} capacitor is larger, briefly $u_{Ci+1} > u_{Ci}$, the balancing current flows from C_{i+1} over the clamping diode and inductor to C_i. The process follows the equivalent circuit of Fig. 3(d). When switch $S_{(i+1)2}$ is turn off and $S_{(i+1)1}$ on, the clamping diode is reverse-biased and the inductor current decays to zero with a rate of $\frac{di}{dt} = \frac{-(V_{C1}+V_{\mathrm{fd}})}{L}$.

The energy transfer continues until the capacitor voltages are equalized. As a result of the vanishing voltage difference, the inductor current will be zero. Typical waveforms of the clamping current and capacitors' voltages are shown in Fig. 5 (a). The following analysis ignores the forward voltage drop of the diodes and switches. With a parallel connection between the two modules as shown in Fig. 3, the simplified circuit is a series RLC circuit, as shown in Fig. 5(b), where $C_e = \frac{1}{2}C_i = \frac{1}{2}C_{i+1}$, $U_{\mathrm{diff},i} = U_{i+1} - U_i - V_{\mathrm{fd}} - V_{\mathrm{sw}}$, and $R = 2r_C + 2r_S + r_L$ are the parameters of the simplified circuit. Solving the resulting second-order equation

$$\frac{d^2u_{\mathrm{diff}}}{dt^2} + \frac{R}{L}\frac{du_{\mathrm{diff}}}{dt} + \frac{1}{LC_e}u_{\mathrm{diff}} = 0, \qquad (1)$$

leads to two roots per

$$P_{1,2} = \frac{-R}{2L} \pm \sqrt{\left(\frac{R}{2L}\right)^2 - \frac{1}{LC_e}} \quad . \qquad (2)$$

Based on (2), two scenario are possible:

Scenario 1: $R \geq 2\sqrt{\frac{L}{C_e}}$ (nonoscillatory, overdamped charge equalization)

Scenario 2: $R < 2\sqrt{\frac{L}{C_e}}$ (damped oscillation with frequency of $\sqrt{\frac{1}{LC_e} - \left(\frac{R}{2L}\right)^2}$)

Due to small equivalent resistances, the normal operation of the system is usually underdamped. To reduce the power loss due to oscillation, on the other hand, it is better to keep the system close to the under-damped threshold ($R < 2\sqrt{\frac{L}{C_e}}$). From (1), the balancing current can be derived as

$$i(t) = Ae^{-\alpha t}\sin(\omega_d t), \qquad (3)$$

where $\alpha = \frac{R}{2L}$, $\omega_0 = \frac{1}{\sqrt{LC_e}}$, $\omega_d = \sqrt{{\omega_0}^2 - \alpha^2}$, $i(0) = 0$, V_{diff} is the initial voltage difference between modules, $\frac{di(0)}{dt} = \frac{V_{\mathrm{diff}}}{L}$, and the current amplitude is $A = \frac{V_{\mathrm{diff}}}{L(\omega_d - \alpha)} = \frac{V_{\mathrm{diff}}}{\sqrt{\frac{L}{C_e}\frac{R^2}{4} - \frac{R}{2}}}$.

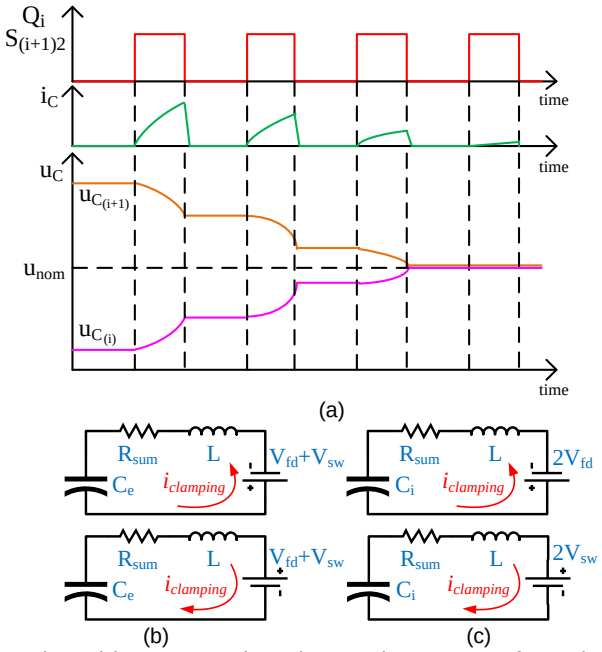


Fig. 5. (a) Representative voltage and current waveforms during balancing; (b) simplified equivalent circuit with the two capacitors in parallel; (c) simplified equivalent circuit when $S_{(i+1)2}$ is switched off

At the end of a balancing period, during which $S_{(i+1)2}$ and Q_i are turned off, two conditions are possible and shown in Fig. 5(c). In case of $u_{C_{i+1}} > u_{C_i}$, the current tails off to zero by discharging into C_i through free-wheeling diodes. In case of $u_{C_i} > u_{C_{i+1}}$, turning Q_i off discharges the inductor into the IGBT snubber and parasitic capacitances as well as C_i so that the inductor current decays. The current path of the inductor during Q_i turn-off is shown in Fig. 6. Additionally, Section II-D investigates the snubber specifications in more detail.

The system is normally underdamped. Therefore, the maximum balancing current ($i_{\max}$) is less than A.

$$i_{max,1} < \frac{V_{\mathrm{diff}}}{\sqrt{\frac{L}{C_e}\frac{R^2}{4} - \frac{R}{2}}} \qquad (4)$$

Furthermore, in case of a switching frequency beyond fundamental switching, the inductor current never gets even close to the peak value. Assuming the voltage difference of the two capacitors is constant during a switching cycle, the inductor peak current limit can be calculated using

$$i_{\max,2} < \frac{V_{\mathrm{diff}}}{L} D_{\max} T_s, \qquad (5)$$

where it is possible to consider $D_{\max} = 1$ as the worst-case scenario.

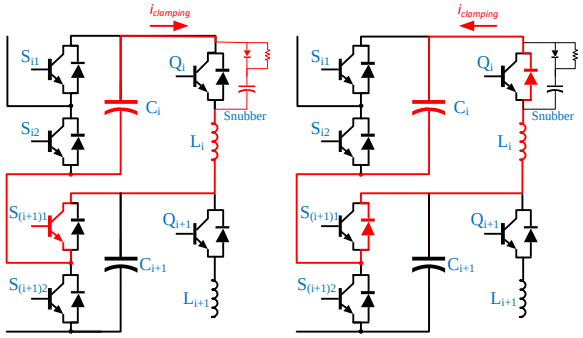


Fig. 6. Current path of the clamping inductor when Q_i and $S_{(i+1)2}$ are turned-off

Equations (4) and (5) can be used to select a suitable inductor value that can limit the peak current to a desired value per

$$L \geq \min\left(\left[\left(\frac{V_{\text{diff,max}}}{i_{\text{rated}}}+\frac{R}{2}\right)^2+\frac{R^2}{4}\right]C_e, \frac{V_{\text{diff,max}}\times T_s}{i_{\text{rated}}}\right). \quad (6)$$

In addition to limiting the current spikes, a larger inductor value reduces the oscillation frequency per $f_{\text{osc}}=\frac{1}{2\pi\sqrt{LC_e}}$ and the power loss caused by the oscillations. On the other hand, a larger inductor reduces the speed of balancing, increases the inductor cost as well as voltage difference [35]. Therefore, the inductor value should be designed considering the following.

The lower limit of the inductor is defined according to (6), while the switching and fundamental frequencies of the system limit the upper boundary. Since the modules are balanced during their bypass state, the average time duration that a module remains bypassed should be higher than the oscillation time constant, to ensure a balanced operation. The average time share of the bypass states of upper and lower arm are respectively calculated based on

$$\overline{T_{b,U}}=\frac{k_U\times\bar{m}_U}{f_0}, \quad (7)$$

$$\overline{T_{b,L}}=\frac{k_L\times\bar{m}_L}{f_0}, \quad (8)$$

where k_U and k_L are coefficients that relate to modulation methods with a value between zero and one, $\bar{m}_U$ and $\bar{m}_L$ are average modulation indices for upper and lower arm, and f_0 is the fundamental frequency of the output voltage. For the nearest-level and conventional phase-shifted carrier modulations, (k_U and k_L) = 1, and $\bar{m}_U=0.5, \bar{m}_L=0.5$.

Assuming $\overline{T_{b,U}}=\overline{T_{b,L}}=\overline{T_b}$, in order to ensure balanced operation, the inequality

$$5\times\left(\frac{2L}{R}\right)\leq\overline{T_b} \quad (9)$$

should be fulfilled, where five times the system time constant is considered as the limit to ensure complete balancing during one cycle of the output voltage. Through simple manipulation the upper boundery for the inductor can be calculated as

$$L\leq\frac{\overline{T_b}\times R}{10}. \quad (10)$$

With a known inductor value, the current rating of the clamping switch ($i_{\text{rated}}\geq i_{\max}$) can be calculated as

$$i_{\text{rated}}\geq\min\{(4),(5)\}. \quad (11)$$

The current rating of Q_i can be orders of magnitude lower than that of the power switches (here less than 1/20$^{\text{th}}$ of the phase current amplitude); however, the voltage ratings of Q_i and its anti-parallel diode are similar to the main power switches. It is also possible to first select a suitable current rating for the switch and then design the required inductor limits using (6) and (10). Furthermore, the anti-parallel diodes prevent any negative voltage on the IGBTs.

B. *Power Loss Analysis*

The power losses of the topology contain the usual contributions of *a*) switching loss (P_{SW}) and *b*) conduction loss. The conduction loss includes balancing loss associated with parallelization ($P_{\text{cond,par}}$) and other resistive losses caused by the main arm current ($P_{\text{cond},I_{\text{arm}}}$). Although the value of $P_{\text{cond},I_{\text{arm}}}$ is widely independent of the switching frequency and depends only on arm current, P_{sw} and $P_{\text{cond,par}}$ strongly rely on the switching frequency.

i. Conduction Loss

The conduction loss can be derived from (1) as

$$P_{\text{cond}}=P_{\text{par}}(f_{\text{sw}},I_{\text{arm}})+P_{I_{\text{arm}}}(I_{\text{arm}}). \quad (12)$$

Considering constant load and assuming identical modules, the second term of the conduction loss would be a constant and can be easily calculated. $P_{I_{\text{arm}}}$ of one arm can be calculated as [43] per

$$P_{I_{\text{arm}}}=n\left(P_{S_U}+P_{D_U}+P_{S_L}+P_{D_L}\right)+P_{R_{\text{arm}}}, \quad (13)$$

where n is the number modules in each arm, P_{S_U} refers to the average conduction loss in the upper switch of the main half-bridge, and P_{S_L} to the average conduction loss in the lower switch of the main half-bridge. Similarly, P_{D_U} and P_{D_L} denote the average conduction loss in the anti-parallel diodes of the main upper and lower switches of the modules. $P_{R_{\text{arm}}}$ is the conduction loss of the parasitic resistance of the arm inductor. $P_{I_{\text{arm}}}$ only depends on the load current and modulation index, and it is independent of the switching frequency ($P_{I_{\text{arm}}}=\text{constant}=K_1$).

Parallelizing two module capacitors with a voltage difference can result in energy losses. It mostly appears as resistive loss along the current path [44]. The energy loss due to parallel connection of two capacitors with different voltages follows

$$E_{\text{Loss,parallel}}\approx\frac{1}{4}C\,\Delta v^2=\frac{C}{4}\left(\frac{I\,\Delta t}{C}\right)^2. \quad (14)$$

Variable Δt is the duration for which one module is connected in series while the other one is still in bypass state. Such conditions, when one module is charging/discharging while the other one is not, can lead to accumulating imbalance. Although Δt is variable during the voltage cycle, one can calculate the effective duration ($\bar{\tau}$) using the difference in the duty cycles of the modules (for a detailed derivation, please see the online supplement). The value of $\bar{\tau}$ can be calculated using

$$\bar{\tau}=\frac{\delta}{f_{\text{sw}}}\frac{m}{2}, \quad (15)$$

where f_{sw} is the swithing frequency, m is the modulation index, and $\delta=\sqrt{\frac{1}{2}\left[\left(1-\cos\left(\frac{2\pi}{N_{\text{arm}}}\right)\right)^2+\sin^2\left(\frac{2\pi}{N_{\text{arm}}}\right)\right]}$ is a constant. The value of $\bar{\tau}$ is identical for both arms.

Substituting $\bar{\tau}$ with Δt in (14) results in

$$\overline{E}_{\text{Loss,parallel}}=\frac{m^2\delta^2}{16C}\frac{{I_{\text{arm,rms}}}^2}{f_{\text{sw}}^2}, \quad (16)$$

where the RMS of the arm current based on [43] is $I_{\text{arm,rms}}=\frac{I_P}{2}\sqrt{\frac{1}{k^2}+\frac{1}{2}}$, I_P the amplitude of the phase current, and $k=\frac{2}{m\cos\varphi}$. Therefore, the average energy loss for one arm amounts to

$$P_{\text{loss,Par}}=K_2\frac{I_P^2}{{f_{\text{sw}}}^2}, \quad (17)$$

where coefficient $K_2=\frac{n}{64C}\left(\frac{1}{k^2}+\frac{1}{2}\right)\delta^2$.

ii. Switching Loss

The energy loss due to one switching action can be calculated according to the literature [43] as

$$E_{\text{sw,module}}=\frac{1}{2}V_{\text{m}}I_{\text{m}}(t_{\text{on}}+t_{\text{off}})+E_{\text{snub}}, \quad (18)$$

where I_{m} and V_{m} are the switch instantaneous voltage and current. E_{snub} is the snubber loss and can be calculated following

$$E_{\text{snub}}=0.5C_{\text{eq,S}}\,V_{\text{m}}^2, \quad (19)$$

where $C_{\text{eq,S}}$ is the equivalent capacitance of the snubber circuit and the parasitic capacitance of the switch (see Subsection II-D). Assuming balanced operation, the module voltage can be considered constant and the RMS value of the arm current can replace the

instantaneous current value to calculate the average energy loss of one arm per

$$P_{\mathrm{sw}} = K_3 f_{\mathrm{sw}} I_P + K_4 f_{\mathrm{sw}}, \tag{20}$$

where $K_3 = \frac{1}{2}\sqrt{\frac{1}{k^2}+\frac{1}{2}}V_{\mathrm{dc}}(t_{\mathrm{on}}+t_{\mathrm{off}})$ and $K_4 = 0.5C_{\mathrm{eq,S}}V_{\mathrm{m}}^2$ are constants. The value of K_3 in the literature is about 1.1-times the value here, K_4 at least two times of the value here. The reason is the higher number of semiconductors in [35].

iii. Optimal Switching Frequency

The total power loss can be calculated by combining all the previously calculated loss components per

$$P_{\mathrm{total}} = K_1 + K_2\frac{{I_P}^2}{f_{\mathrm{sw}}} + K_3 f_{\mathrm{sw}} I_P + K_4 f_{\mathrm{sw}}, \tag{21}$$

where K_1 represents the conduction losses that are independent of the switching frequency (here called $P_{I_{\mathrm{arm}}}$).

Higher switching frequency will result in a better balancing performance. However, increasing the switching frequency also increases the switching loss. Therefore, the trade-off between the power loss and balancing performance should be considered to determine a suitable switching frequency. By differentiating P_{total} with respect to f_{sw}, the optimum switching frequency can be calculated as

$$f_{\mathrm{sw,opt}} = \sqrt{\frac{K_2 I_P^2}{K_3 I_P + K_4}}. \tag{22}$$

C. THD Analysis

The total harmonic distortion (THD) analysis depends only on the number of modules and the modulation method. The added clamping circuit has a negligible effect on the behavior of the MMC from the output point of view, and it is possible to analyze the THD of the voltage with available equations for MMC [45, 46]. The fundamental amplitude of the PSC modulation follows

$$A_1 = \frac{8V_d}{\pi}\sum_{i=0}^{\left(\frac{f_{\mathrm{sw}}n}{2f_1}\right)}(-1)^j\cos(\alpha_i), \tag{23}$$

where $0 < \alpha_1 < \alpha_2 < \ldots < \frac{\pi}{2}$ are the switching angles and $j = \begin{cases}1 \text{ positive step}\\ 0 \text{ negative step}\end{cases}$.

Comparing the acquired amplitude with the resulting step voltage waveform, it is possible to calculate the THD of the voltage

$$THD = \frac{\sqrt{\frac{2}{\pi}\sum_{i=0}^{\left(\frac{f_{\mathrm{sw}}N}{2f_1}\right)}\left(\int_{\varphi_i}^{\varphi_{i+1}}(V_{i,d}-A_1\cos(\varphi))d\varphi\right)^2}}{A_1}, \tag{24}$$

where $\varphi_0 = 0$, and φ_i is the switching instance. As can be seen, THD is widely independent of the balancing operation.

D. Snubber Design Discussion

The main challenge of this approach is to limit the voltage rise on the snubber capacitor. The peak voltage amplitude can be estimated using $\mathrm{V}_{\mathrm{m,peak}} = \sqrt{\frac{(L_i I^2)}{C_{\mathrm{eq,S}}}+V_{\mathrm{m,rated}}^2}$, where I is the inductor current at the time of turning Q_i off, $C_{\mathrm{eq,S}}$ is the equivalent capacitor equal to $C_{\mathrm{eq,S}} = C_{\mathrm{S}} + C_{\mathrm{CE,IGBT}}$, and $V_{\mathrm{m,rated}}$ is the module rated voltage. Considering 5 % of the rated voltage as the maximum permissible voltage rise, the snubber should follow

$$C_{\mathrm{S}} = \frac{(L_i I^2)}{0.1025V_{\mathrm{m,rated}}^2} - C_{\mathrm{CE,IGBT}}. \tag{25}$$

After the inductor current has reached zero and Q_i is turned off, C_{S} is discharged and reset through the snubber resistor R_{S}, L_i, and switch–diode set $S_{(i+1)1}$ into C_i. Therefore, the value of R_{S} should be low enough that the excess charge of C_{S} is balanced with C_i while Q_i is off. Hence, the time constant of the formed RC circuit should be on the order of or less than the minimum off duration of Q_i (here assumed 3 % of a switching cycle). The value of R_{S} should be also high enough to limit the discharge current in Q_i during turn-on. Hence, R_{S} is calculated per $\frac{V_{\mathrm{m}}}{I} \le R_{\mathrm{S}} \le \frac{0.03T_{\mathrm{s}}}{2C_{\mathrm{S}}}$ and the power rating of R_{S} can be approximated with $0.6f_{\mathrm{sw}}C_{\mathrm{s}}V_{\mathrm{m}}^2$. The calculated snubber values in the simulation section are based on the SEMiX854GB176HDs model from Semikron.

III. Simulation Results

To analyze the behavior of the proposed clamping circuit, a three-phase model of the same topology depicted in Fig. 2(b) is simulated in MATLAB/Simulink. To generate the switching pulses a typical phase-shifted carrier (PSC) method is utilized, where the phase-shift of each carrier signal (ϕ_i) compared to the output voltage is

$$\phi_i = \frac{(i-1)\times 2\pi}{n}, \tag{26}$$

where ϕ_i is the intial phase shift of the i^{th} module in the arm [47]. Also the upper and lower arms' modulation references are generated based on (27) and (28) with the modulation index of 0.95, respectively.

$$ref_U = \frac{1-m\times\sin(\omega t)}{2} \tag{27}$$

$$ref_L = \frac{1+m\times\sin(\omega t)}{2} \tag{28}$$

The switch–diode pair uses SEMiX854GB176HDs specifications from Semikron. Other parameters of the simulated system are listed in Table II. The presented snubber design discussion and the system parameters in Table II recommend a 20 nF snubber capacitor on top of 50 nF parasitic capacitance to limit the voltage rise on Q_i to below 5 % of the rated voltage while R_S should be in the range between 36 Ω and 150 Ω. In simulations, $R_S = 120\ \Omega$.

The three-phase output voltages of the simulated MMC with and without the proposed clamping circuit are presented in Fig. 7(a). Additionally, the THDs of the voltages in both cases in Fig. 7(b) show that the clamping circuit has no negative effect on the behavior of the system from the output point of view.

TABLE II
SYSTEM PARAMETERS

		Simulation	Experiments
Modul number (per arm)		20	4
Rated power (per arm)		3.6 MVA	1 kVA
DC link voltage		24 kV	120 V
Grid Frequency		50 Hz	50 Hz
Modulation technique		PSC	PSC
Switching Frequency		5 kHz	10 kHz
Modulation index (m)		0.95	0.95
Switch parameters	Model	SEMiX854GB176HDs	IPT015N10N5
	V_{CE} [1]	1–2.5 V	–
	R_{CE}	2 mΩ	1.5 mΩ
	$t_{\mathrm{on}}+t_{\mathrm{off}}$	1.7 µs	–
Module capacitor		6 mF	4.4 mF
Decoupling inductors		10 µH	7.5 µH
Decoupling inductor resistance		0.1 mΩ	0.5 mΩ
Arm inductor		10 mH	1.5 mH
Inductor resistance		50 mΩ	40 mΩ
Implementation		MATLAB	sbRIO9627

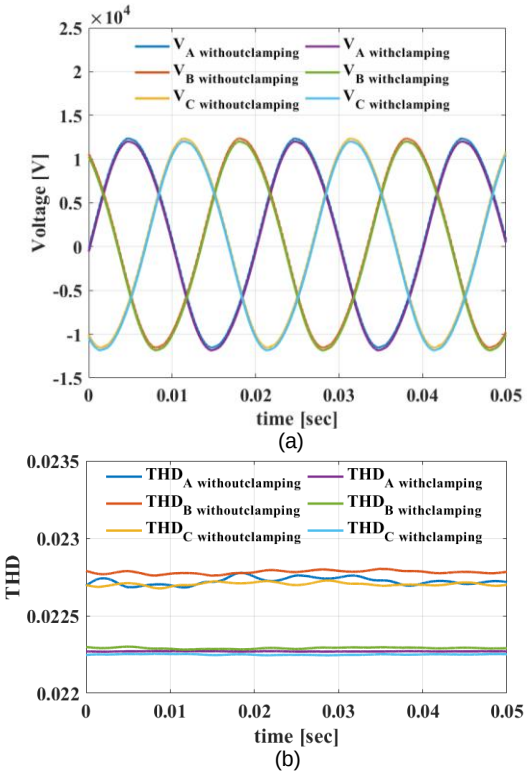


Fig. 7. (a) Three-phase output voltages with and without clamping circuit; (b) THDs of the output voltages

To verify the balancing performance of the proposed topology, the system is simulated with similar parameters, but the modules in one arm are intentionally unbalanced in the beginning of the simulation and the capacitor waveforms are shown in Fig. 8(a). In another scenario, the capacitance and self-discharge rate of some of the modules are changed to simulate parameter spread due to manufacturing tolerance and aging for different modules. A higher self-discharge is simulated using a resistance in parallel to some of the modules. Similarly, the capacitors are unbalanced due to the above-mentioned tolerances during the initialization. Table III lists the modifications in the system parameters for severe mismatch between submodules. Figure 8(b) shows the simulation result for the voltage of the modules. Although the voltages are randomly unbalanced at the beginning, all the voltages converge to the rated value after few cycles.

The simulation results in both cases and verify the suitable performance of the proposed topology. The voltage difference between the modules, even in the case of severe unbalance, is limited to 0.8 % of the rated value.

Figure 9 shows the system power loss curves based on the

TABLE III
MODIFIED SIMULATION PARAMETERS FOR SEVERE UNBALANCE

Simulations		Experiment	
Modified Modules	ΔC or Parallel Resistors	Modified Modules	ΔC or Parallel Resistors
2, 5	$0.3 \times C_{\mathrm{SM}}$	SM_{3U}, SM_{4L}	$-0.15 \times C_{\mathrm{SM}}$
4, 10, 14, 15, 16, 19, 20	$0.15 \times C_{\mathrm{SM}}$	SM_{4U}, SM_{3L}	$0.15 \times C_{\mathrm{SM}}$
1, 6, 8, 9, 12	$-0.3 \times C_{\mathrm{SM}}$	SM_{4L}	4 kΩ
11, 17	$-0.15 \times C_{\mathrm{SM}}$	SM_{3U}	58 kΩ
1, 20	1.5 kΩ	–	–
10	1 kΩ	–	–

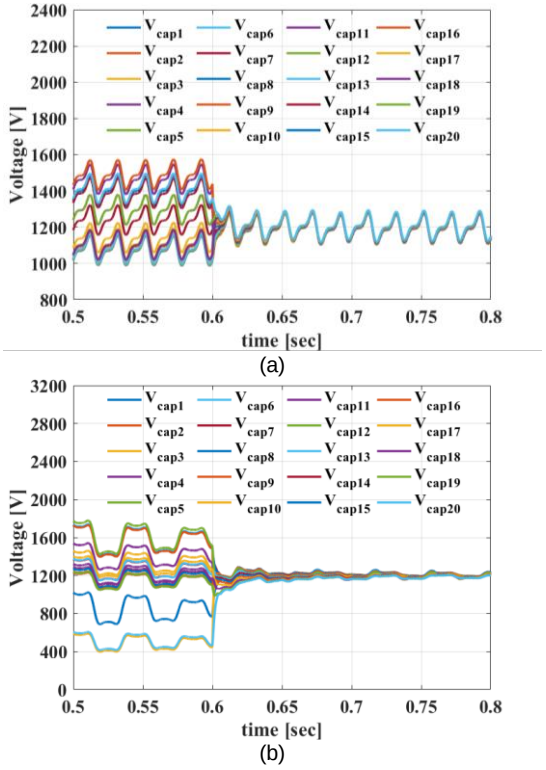


Fig. 8. Simulation results with unbalanced : (a) different initial voltages; (b) different capacitance and self-discharge rates

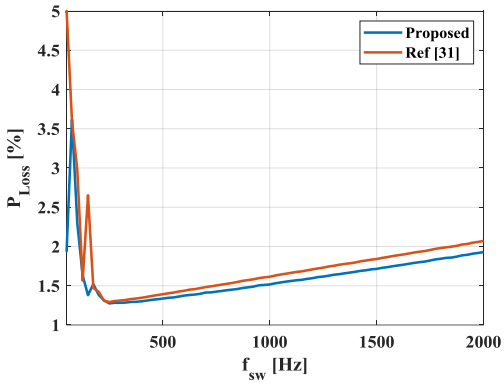


Fig. 9. Power loss in dependence of the switching frequency

switching frequency for the proposed topology and the one presented in [35]. As can be seen, the proposed topology benefits from generally lower power losses. The optimum switching frequency based on Fig. 9 is 250 Hz, while the optimum switching frequency according to (18) is 244 Hz. The power loss analysis is

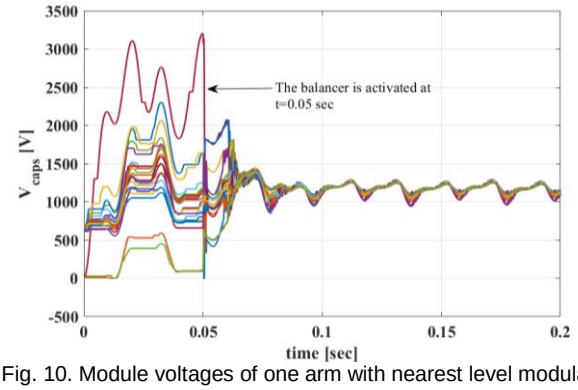


Fig. 10. Module voltages of one arm with nearest level modulation

derived under the assumption of sinusoidal output voltage and current, which results in only one extremum point in (20). Other extremum points in Fig. 9 follow from the abnormal behavior of the PSC modulation at excessively low switching frequencies, where the PSC modulation cannot achieve a high-quality sinusoidal output voltage due to poor distribution of the carriers with respect to the arm modulation reference. The resultant low-frequency harmonics increase the voltage THD and affect the output power as well as the efficiency, particularly when the switching frequency is not an integer multiple of the output voltage frequency [45, 46]. The optimum switching frequency increases as parameter mismatch between the modules grows or lower capacitances are used in the modules. Additionally, during normal operation, the power rating of the balancing path is less than 0.3 % of the system power.

We investigated the balancing behavior of the system for low-frequency modulation techniques with the nearest-level modulation method proposed in [5]. Fig. 10 presents the corresponding result. The balancing system is activated at t=0.05 sec. Before the activation of the balancing circuit, the capacitor voltages start to diverge. However, when the balancing operation starts, all the voltages converge to the nominal value.

IV. Experimental Validation

To validate the simulation and analysis, we have constructeed an laboratory prototype, as shown in Fig. 11. The parameters of the prototype are given in Table III. Using (6) and (10), the clamping inductor value is selected between 3 µH and 10 µH. Passing a wire through a toroidal ferri-magnetic core results in 7 µH with minimum resistance [48]. The module capacitance comprises low-ESR ceramic in parallel with electrolyte capacitors. The control is implemented in Labview with a NI-sbRIO 9627 development board from National Instruments. There are four modules in each arm, which can generate up to five-level output voltage using PSC modulation. Similar to the simulations, two scenarios are shown in Fig. 12. The output voltage of the converter during normal operation and severe mismatch of module parameters are presented in Fig. 12 (a) and (b), respectively. Table III lists the modified components of the system in this scenario. Furthermore, Fig. 12(c) shows the measured arm currents in the case of mismatch among modules imbalance.

The imbalanced module voltages are visualized in Fig 13(a). The voltages converge to the rated value imidiately after starting the switching the modules. The balancing operation with a spread of 50% lasts less than 30 ms. In Fig. 13(b) and Fig. 13(c), voltages of the lower arm modules' are shown for a normal condition and severe mismatch between the modules as listed in Table III,

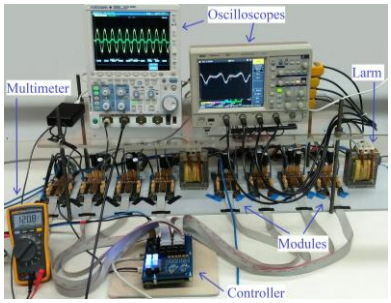
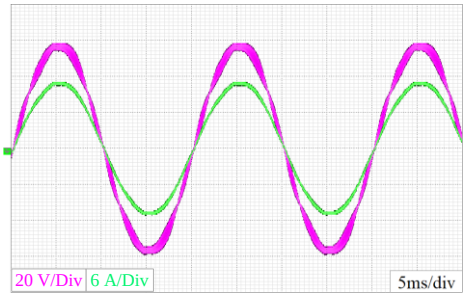
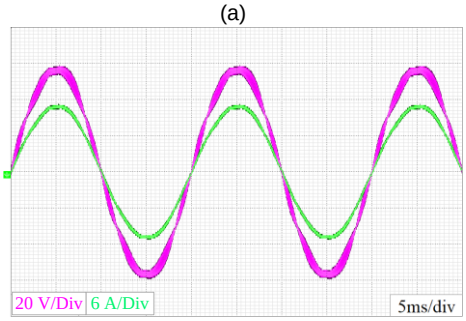


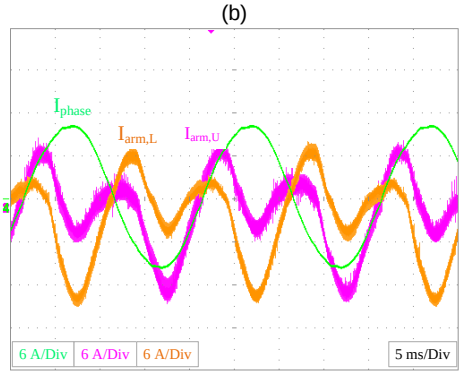
Fig. 11. Laboratory testbench



(a)



(b)

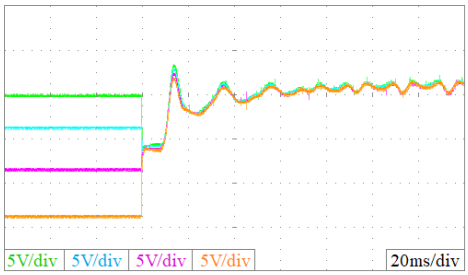


(c)

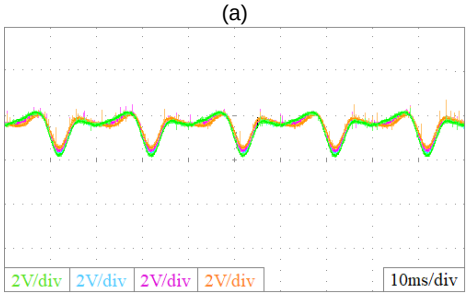
Fig. 12. Measured output voltage and output current of the lab prototype with the clamping circuit: (a) normal operation (b) unbalanced situation (c) arm and output current waveforms

respectively. Although the voltage variation increased, the system can achieve balanced operation and the maximum voltage difference is limited to less than 1.5 %. Therefore, the proposed system can achieve sensorless operation under severe mismatch between an arm's modules.

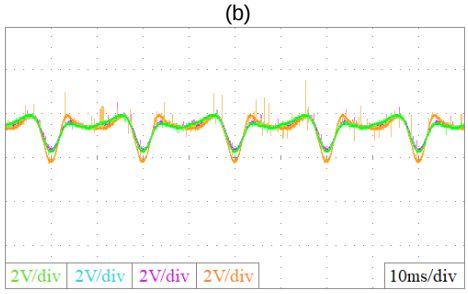
Fig. 14 depicts the current of the clamping inductor and the voltage across Q_i during balancing operation of the third and the fourth module of the lower arm. As can be seen, the snubber demagnetizes the inductor so that there are no overt spikes while the coil current decays after the two modules are balanced. Comparing Figs. 5(a) and 14 reveals several differences. Although in Fig. 5(a) the duty cycle of Q_i, is kept constant for illustrative purposes, the duty cycle is constantly varying according to (27) and (28) in practice. Therefore, the convergence speed depends also on the duty cycle of switches $S_{(i+1)2}$ and Q_i. The second differentiable factor is balancing speed. In Fig. 5(a), we provide an intuitive representation of balancing in just a few cycles. However, the process of balancing is more gradual because of high-switching frequencies. Furthermore, Fig. 14 shows the collector–emitter voltage of Q_i, which is complementary to the gate signals shown in Fig. 5(a). Therefore, the modules in Fig. 5(a) are balanced when the gate signal of Q_i turns high and in Fig. 14 when



(a)



(b)



(c)

Fig. 13. Experimental Results: (a) initial voltage unbalance; (b) module voltages when normal operation; (c) module voltages when severe mismatch between the modules

the voltage across Q_i decays to zero. Finally, the waveforms in Fig. 5(a) isolate the module pair from the impact of other modules on the balancing process for explanation, while in the experiment the modules are highly coupled to each other, which can affect the balancing waveforms. It is noteworthy that the clamping circuit is designed for small imbalances (e.g., less than 1.5 %) that occur during normal operation (e.g., between subsequent switching cycles). Major fluctuations, which we intentionally created by a 10 % voltage imbalance between the two neighboring modules, the inductor faces a substantial magnetization current, which should be accounted for in the design of the magnetics since it can behave nonlinearly as visible here during the first three switching cycles.

V. Conclusion

This paper proposed an improved clamping topology for MMCs with half-bridge submodules. Sensorless operation and improved efficiency are two salient benefits of the proposed topology. Moreover, as compared with other sensorless balancing solutions, the proposed one requires fewer components and no extra control, which allows the proposed technique in principle even to be added to existing MMC systems through retrofitting.

Table I presents a general comparison of the proposed method with other solutions. In summery, the proposed method provides particular advantages for high-power low- and medium-voltage applications with fast dynamic responses.

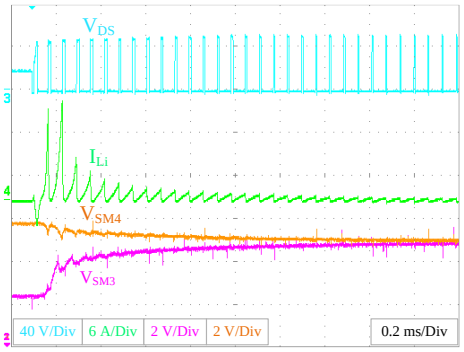


Fig. 14. Clamping circuit voltage and current waveforms

Simulation and experimental results clearly validate the effectiveness of the proposed clamping topology. The voltages of the modules remain balanced within tight boundaries even when capacitances and self-discharge parameters are significantly different across modules. In all cases, the maximum voltage difference is limited to be less than 1 % or 1.5 % of the rated voltage for simulations or experiments, respectively. In addition, the proposed clamping topology does not affect the normal operation of MMCs in terms of load operation and voltage THDs.

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Supplement I: Complete derivation of effective duration $\bar{\tau}$

Variable Δt denotes the duration for which one module is connected in series while the other one is still in bypass state. Such conditions, when one module is charging/discharging while the other one does not, can lead to accumulation of imbalance. Although Δt is variable during the voltage cycle, we can calculate the effective duration ($\bar{\tau}$) using the difference in the duty cycles of the modules. The duty cycles of the two modules can be written as

$$D_1(t) = \frac{1+m\sin(\theta)}{2} \times T_{\mathrm{sw}} \tag{1}$$

$$D_2(t) = \frac{1+m\sin(\theta-\varphi)}{2} \times T_{\mathrm{sw}} \tag{2}$$

where $D_1(t)$ and $D_2(t)$ are the average durations that they are connected in series to the arm, φ is the phase shift between two consecutive modules, T_{sw} is the switching period, and m is the modulation index.

For conventional phase-shifted modulation, the phase shift for each module follows

$$\varphi_j = \frac{2\pi\,(j-1)}{N_{\mathrm{arm}}}. \tag{3}$$

Therefore, the phase difference between two consecutive modules is constant and equal to $\varphi = \frac{2\pi}{N_{\mathrm{arm}}}$. The effective value of Δt is the effective time difference between (1) and (2) in one cycle, which is calculated per

$$\bar{\tau} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left(\frac{1+m\sin\theta}{2} - \frac{1+m\sin\left(\theta-\frac{2\pi}{N_{\mathrm{arm}}}\right)}{2}\right)^2 T_{\mathrm{sw}}^2\, d\theta}. \tag{4}$$

Replacing T_{sw} with $\frac{1}{f_{\mathrm{sw}}}$ and some mathematical manipulation, (3) can be rewritten as

$$\bar{\tau} = \frac{m}{2f_{\mathrm{sw}}}\sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left(\sin\theta - \sin\left(\theta-\frac{2\pi}{N_{\mathrm{arm}}}\right)\right)^2 d\theta}, \tag{5}$$

Expanding the $\sin\left(\theta-\frac{2\pi}{N_{\mathrm{arm}}}\right)$ term in (5) results in

$$\bar{\tau} = \frac{m}{2f_{\mathrm{sw}}}\sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left(\sin\theta - \sin(\theta)\cos\left(\frac{2\pi}{N_{\mathrm{arm}}}\right) + \cos(\theta)\sin\left(\frac{2\pi}{N_{\mathrm{arm}}}\right)\right)^2 d\theta}. \tag{6}$$

With further manipulation, (6) results in

$$\bar{\tau} = \frac{m}{2f_{\mathrm{sw}}}\sqrt{\frac{1}{2\pi}\int_0^{2\pi}\left[\sin^2(\theta)\left(1-\cos\left(\frac{2\pi}{N_{\mathrm{arm}}}\right)\right)^2 + \cos^2(\theta)\sin^2\left(\frac{2\pi}{N_{\mathrm{arm}}}\right)\right] d\theta}. \tag{7}$$

The final equation after the integration follows

$$\bar{\tau} = \frac{m}{2f_{\mathrm{sw}}}\sqrt{\frac{1}{2}\left[\left(1-\cos\left(\frac{2\pi}{N_{\mathrm{arm}}}\right)\right)^2 + \sin^2\left(\frac{2\pi}{N_{\mathrm{arm}}}\right)\right]}. \tag{8}$$

For simplicity in representation, the coefficient δ is defined to be

$$\delta = \sqrt{\frac{1}{2}\left[\left(1-\cos\left(\frac{2\pi}{N_{\text{arm}}}\right)\right)^2 + \sin^2\left(\frac{2\pi}{N_{\text{arm}}}\right)\right]}$$

and the effective duration is rewritten as

$$\bar{\tau} = \frac{\delta}{f_{\text{sw}}}\frac{m}{2}. \tag{9}$$

Supplement II: Complete Simulation Results for nearest level modulation

The following presents the simulation results for operation of a three-phase system using nearest level modulation (NLM) with 2*N*+1 voltage levels. The simulated system is identical to the unbalanced system in the manuscript, and Tables II and III of the paper provide its parameters.

Figures 1 and 2 show the output voltage waveforms as well as the THDs of a three-phase system that is heavily unbalanced. However, as can be seen, because of the balancing method, the output voltage is sinusoidal and balanced.

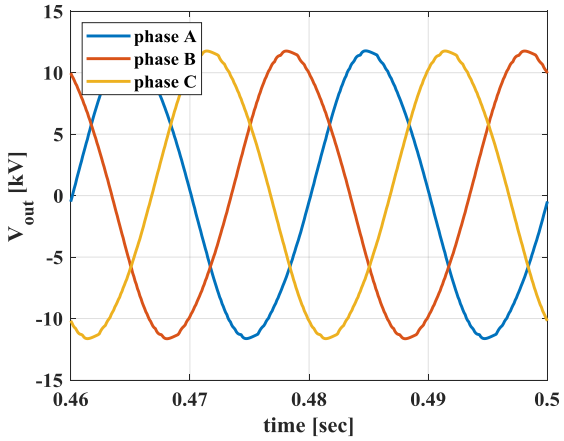

Fig. 1. Output voltage with balancing

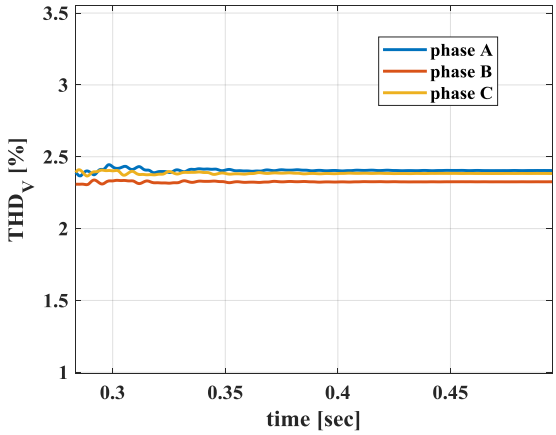

Fig. 2. THD of the output voltage

All the capacitor voltages of one of the phases are shown in Fig. 3. The balancing system is activated at t = 0.05 sec. Before the activation of the balancing circuit, the capacitor voltages start to diverge. However, when the balancing operation starts, all the voltages converge to the nominal value.

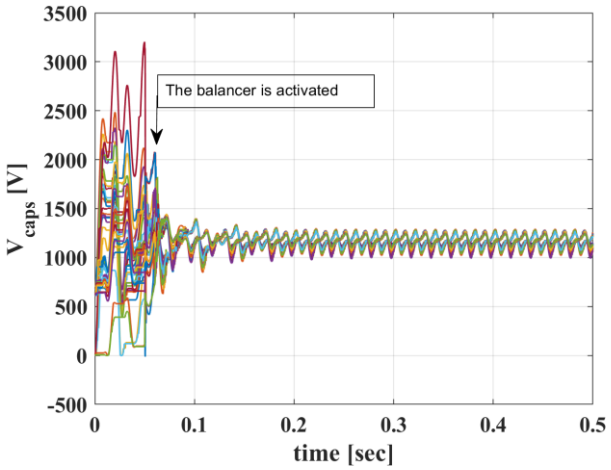

Fig. 3. The module voltages of phase A