

Modular Multilevel Series/Parallel Converter for Bipolar DC Distribution and Transmission

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Abstract—This paper proposes a novel bipolar-type dc system suitable for both distribution and transmission systems based on Modular Multilevel Series/Parallel Converters. The system features decoupled operations of each pole of the bipolar system, being able to operate in both asymmetrical and regenerative modes. This enables two independent dc systems by using a single grid-tied converter. The Modular Multilevel Series/Parallel Converter is based on a three-switch cell configuration and enables a simple balancing mechanism in combination with a wide range of output voltage frequencies. The simple balancing mechanism is the key to enable dc operation and lead to a simpler scalability for different voltage levels. Theoretical studies as well as experimental results are provided to verify and characterize the proposed system.

I. INTRODUCTION

Over the last five years, the annual worldwide addition of renewable power generation capacity outpaced the net installation of conventional generation combined [1]. The growth is so rapid that currently renewable energy accounts for one third of the world's total installed generation capacity. However, some challenges have arisen, given the stability issues in conventional ac grids due the intermittency and variability of these resources [2], [3]. This has motivated the development of active transmission and distribution networks, in order to transmit the power, manage grids, and include distributed energy generation resources with emphasis on fluctuating clean renewable energy [4].

This steep growth of renewables in the generation matrix, the complications for conventional ac grids to integrate them and the growing presence of dc-based consumer equipment motivated studies and development of active dc distribution networks [5]. Among other things, these systems promise

This work was supported in part by the ANID projects: FONDECYT under grant no. 1201344, AC3E (ANID-Basal Project FB0008), SERC-Chile (ANID/FONDAP/15110019) and REDES-PCI no. 190108; in part by the National Science Foundation under grant No. 1608929, the North Carolina Biotechnology Center under grant No. 2016-CFG-8004, a seed grant from the Duke University Energy Initiative, and in part by the Lakehead University SRC NSERC Research Development Fund 2020 under project no. 1467749.

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substantial improvements in terms of cost, efficiency, space, and reliability [6].

In the high-power range, high-voltage direct-current (HVDC) transmission or grids on top of the ac system can provide a robust energy matrix. While HVDC can improve power transmission, *i.e.*, solve problems with capacity, congestion, reliability, and economics, the ac distribution system faces similar issues [7], [8]. Thus, enabled by advances in power electronics and the wide experience with dc-based consumer appliances, dc architectures are also being promoted for the low- and medium-voltage levels [9]. Currently, dc-based equipment is increasing its presence in various kilowatt-scale applications, which can be found in different sectors such as aerospace, automotive, data centers, or marine systems. Such dc-grids may become key elements for a large-scale deployment of distributed generators, allowing increased power capacity, enhanced power quality, and resilience against power surges, disturbances, as well as asymmetrical loads [10].

There are two main structures for implementing a dc distribution grid: unipolar (or monopolar) and bipolar. However, bipolar dc distribution, which resembles the three-phase ac system and uses three wires to generate two different voltage levels, provides a more reliable and flexible alternative to the unipolar dc distribution system [11]. Bipolar dc lines also provide redundancy, keeping the power transfer from collapsing when a line fails, besides allowing to distribute loads to two different regulated voltages [12]. However, if the bipolar system experiences differences in power generation or consumption of the loads connected to the two dc-buses, voltage imbalances can occur, which can severely compromise the system's performance [13]. For these reasons, balancing control becomes essential in bipolar dc systems as the loads on the two buses of the distributed system will differ most of the time [14].

For HVDC grids, the standard bipolar configuration is based on two unipolar symmetrical converters, which are connected in series at the dc side [15]–[17]. With this structure, it is possible to control the voltage of each bus through the dedicated converter, allowing the decoupled operation of the dc terminals regardless the load conditions. However, the operation and control of an independent converter for each dc-bus, affects directly the cost of the whole HVDC bipolar system.

On the other hand, at distribution level, various balancing methods have been proposed for LVDC, covering simple solutions such as the use of two cascaded two-level voltage

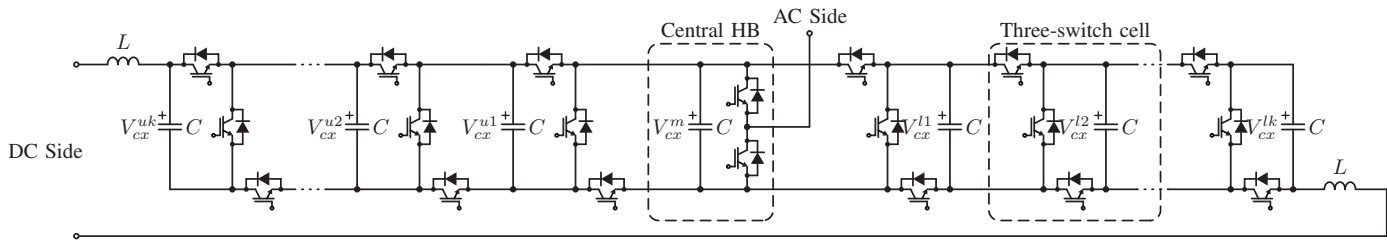


Figure 1. Proposed basic leg (or phase) topology.

source converters (2L-VSC) together with a multi-winding transformer [18], the use of a three-level NPC converter (3L-NPC) with limited asymmetrical load operation [13], or employing additional circuitry acting as voltage balancers [19] or current redistributors [20]. These balancing strategies and auxiliary circuits allow the implementation of bipolar dc distribution systems with the capability of maintaining the operation performance under asymmetries in the dc loads. However, these converters are not able to cover the full spectrum of distribution voltages despite of being able to implement solutions up to 6.6 kV [21]. First, and despite of the existence of 6.5 kV devices, the solutions using 2L-VSC and discrete devices are not cost-effective for powers above 1 MW, mainly due to poor efficiency, larger filter requirements and reduced voltage quality. For larger powers, series-connected arrays of switches are employed, which can even reach transmission level (HVDC light for example), but these solutions still have issues with the voltage sharing phenomenon besides featuring a large device count [22], [23]. The case of the 3L-NPC is similar, given that commercial NPCs reach voltages in the range of 2.2-6.6 kV, within a wider power rating range (3 kW - 50 MW) [24], resulting in a lack of options for most of the MVDC range.

Besides, none of these approaches features a modular structure, which would entail the advantages known from other fields, such as high efficiency and reliability, simple maintenance, reduced manufacturing cost, as well as scalability, and allow the use of the same power topology in both low and high power applications, by merely changing the number of modules in the converter [25], [26].

This paper presents a novel bipolar-type dc system based on the modular multilevel series/parallel converter (MMSPC). The proposed bipolar dc system comprises a three-phase grid-tied converter plus a balancing multilevel leg. This balancing multilevel leg is implemented by the use of a three-switch module, while its ac terminal is connected to the midpoint of the dc bus. The main function of the proposed balancing leg is to overcome the asymmetrical operation of the system, through the redistribution of the dc currents. The latter is enabled by the converter's capacity to operate at low frequencies, in contrast to conventional MMC structures. Also, with this three-switch module configuration, it is possible to alternatively interconnect adjacent modules in series and parallel besides bypassing them. This way, a sensorless voltage balancing strategy is enabled among the modules, thereby reducing the complexity and cost of the balancing algorithm. Moreover, the

proposed bipolar dc system can independently control each of its poles, maintaining the performance under asymmetrical load connections, and operate in regeneration mode as well.

In summary, the main contributions of this paper that can be highlighted are:

- Propose a bipolar-type dc system topology, based on a modular converter structure, which allows high system scalability, so that the same concept can be used in high voltage, as in medium/low voltage applications. The proposed bipolar system must maintain its performance under asymmetric load connections or operate in regeneration mode as well.
- Enable HVDC, MVDC and LVDC bipolar grids through the use of a single grid-tied converter.
- Design a control and modulation strategy for the proposed bipolar-type dc system.

The paper is organized as follows. Section II describes the proposed bipolar dc bus architecture. Section III presents a corresponding control scheme. Simulation and Experimental results are included in Sections IV and V respectively. Finally, Section VI draws the conclusion of the work.

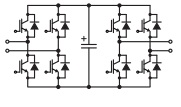
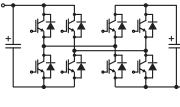
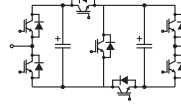
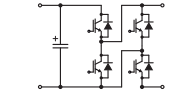
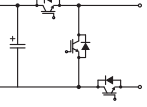
II. BIPOLAR DC BUS ARCHITECTURE

A. Multilevel Leg and Three-Switch Module Configuration

Figure 1 shows the basic leg configuration of the proposed bipolar dc system. This structure is formed by an array of three-switch modules connected in series. Each module is composed of one capacitor C and three semiconductor devices as displayed in Fig. 1. The configuration provides four terminals for interfacing the adjacent modules, which along with the appropriate switching signals, enables four equivalent states. These states are displayed in Fig. 2, where depending on the location of the cell, two different ways of bypassing the cells are available (positive or negative arm). Additionally, the cell can be connected in series with the branch, or alternatively in parallel with the adjacent module.

Then, each phase will interface the ac output terminal through a half-bridge module located at the center of it. This center module allows symmetrical operation between the upper and lower converter arms for the intended system [31]. In Figure 3 the two switching states for this cell are displayed. Their effects depend on the polarity of the output voltage and either connects the cell capacitor in series to the leg output or bypasses it. Finally, similar to conventional modular multilevel converters (MMCs), phase comprises the arm inductors L which suppress switching ripple and inrush currents that may

Table I
MMSPC MODULES COMPARISON

Features	Back-to-back Full Bridge (B2B-FB) [27]	Double Full Bridge (2FB) [28]	Semi Full Bridge (SFB) [29], [30]	Double Half-Bridge (2HB) [31], [32]	Three-switch cell (TS) [33]
Power circuit					
Number of Semiconductors	8	8	7	4	3
Number of Levels	3	3	3	2	2
DC-fault block capability	Yes	Yes	Yes	No	No
Semiconductor power rating	Low	Low	Low	High	High

arise between the cell voltages and the dc-link. Note that these inductances could be either concentrated at the end of the arms, or distributed among the cells, to suppress current spikes that may appear during parallelization, especially when the number of modules is larger than ten, and the possibility of voltage mismatch is larger [31], [34], [35].

Among the main benefits of the proposed structure is related with the voltage fluctuations in the cell capacitors. In conventional MMCs, the positive and negative arm modules experience low-frequency capacitor voltage fluctuations, which are in opposite phase. These fluctuations have severe effects on the converter reliability and operation, and limit MMC applications above the rated output frequency only [36]. The possibility of parallelizing module capacitors, even when they are in different arms, virtually eliminates these effects, regardless the output frequency. This cancellation of voltage fluctuations enable the MMSPC to operate in a wide frequency range (from zero included), hence allowing the use of it at the dc side. Furthermore, the parallel connection equalizes the current flowing through the module capacitors involved in it and aims to reduce their voltage differences, hence facilitating the capacitor voltage balancing strategy. The simpler balance in contrast to conventional MMCs is a key feature of the MMSPC, as it could represent a strong alternative to this well-established converter in various applications. Considering the benefits for voltage balancing, the modulation scheme proposed will alternate series and parallel states for the generation of the output waveform. Bypassing states are applied only in case there is a module failure.

Several MMSPC modules can be found in the literature [27]–[31]. All these topologies provide the option to connect modules in series, bypass or parallel. However, these modules have some operational differences that affect the coherence of their use in different systems. Table I summarizes some operational aspects of five different types of MMSPC modules. Table I compares the most relevant modules available: the back-to-back full bridge (B2B-FB) [27], the double full bridge (DFB) [28], the semi-full bridge submodule [29], the double half bridge (DHB) and the three switch (TS) submodules. The first two options use 8 semiconductors, the cell proposed in [29] reduces this number in one, while the concept in [36] halves this number, compared with the 3 switches featured

in this proposal and introduced in [33]. However, the B2B-FB, DFB and SFB submodules can create three voltage levels, while the DHB and TS ones only generate 2 voltage levels. Another benefit of the modules with a high number of semiconductors is the fact that at each time two semiconductors are in parallel, cutting the current ratings in half. Furthermore, their ability to generate a negative voltage level also provides them with a means to block dc faults. Additionally, the increased number of voltage levels allows competing with comparable implementations of MMCs with HB modules [28], [29]. On the other hand, the B2B-FB, DHB and TS cells allow the parallel connection of the entire array comprising the phase, while the DFB and SFB only allow the parallel connection between two neighboring cells, which enables a more focused balance, but limits system scalability. Finally, all these modules can integrate differential-mode chokes, in order to mitigate the current peaks when connecting two modules in parallel that present a voltage unbalance. The integration of these components allows adding a degree of freedom in order to achieve an optimal operation considering trade-off among the value of the total capacitance of the modules, the switching frequency and the size of the differential-mode chokes [32], [37].

As mentioned earlier, this work will focus in the application of the MMSPC to bipolar dc distribution and transmission systems. The scalability and modularity of its structure, allows this converter to cover a wide spectrum of applications from LVDC to HVDC as it will be illustrated in the following section.

B. Configuration of Bipolar DC System with Grid-Tied Multilevel Converter

Once the structure of the balancing multilevel leg has been presented, the topology of the grid-tied converter is discussed. The selection of the topology of the grid-tied converter is defined by several technical and economical aspects, but fundamentally is related to the power and voltage ranges to which the system will be operating, as shown in Fig. 4. At distribution level, bipolar configurations based mostly on 2L-VSC and 3L-NPC type converters are used with the aid of voltage balancers and current redistributors [9], [10], [13], [19], [20]. However, these solutions are mainly suited for

Table II
COMPARISON OF DC BIPOLAR DISTRIBUTION TOPOLOGIES

Topology	Cascaded 2L-VSC [20]	2L-VSC with voltage balancer [10]	3L-NPC with voltage balancer [13]	Proposed bipolar system based on MMSPC
No. semiconductors.	12	12	16 and 8 Diodes	$3N-1+6$ (*) - $3N-1+12$ and 6 diodes (**)
Topology configuration	2 indept. 2L-VSC plus a multi-winding transformer	One 2L-VSC plus a dc current redistributor	One 3L-NPC plus an additional leg	(*) Grid-tied converter based on 2L-VSC plus a proposed balancing multilevel leg (**) Grid-tied converter based on 3L-NPC plus a proposed balancing multilevel leg
Scalable/Redundancy	No/No	No/No	Yes/No	Yes/Yes
Filter expense	High	High	High	Low

Table III
COMPARISON OF DC BIPOLAR TRANSMISSION TOPOLOGIES

Topology	LCC-HVDC [38]	VSC-HVDC [39]	Hybrid Bipolar HVDC [40]	Proposed bipolar system based on MMSPC
Topology configuration	2 indept. LCC plus a multi-winding transformer	(†)2 indept. VSC based on HVDC-Light (‡)2 indept. VSC based on MMC	One LCC plus a VSC (each converter controls one dc-bus independently)	(*) Grid-tied converter plus balancing multilevel leg based on proposed basic leg (**) Grid-tied converter based on MMC plus a proposed balancing multilevel leg
High Voltage range	$\pm 800/1000\text{KV}$	$\pm 200\text{KV}$	$\pm 500\text{KV}$	$\pm 200\text{KV}$
Filter expense	High	Low	Low	Low
Decoupled control of active and reactive power	No	Yes	Yes	Yes

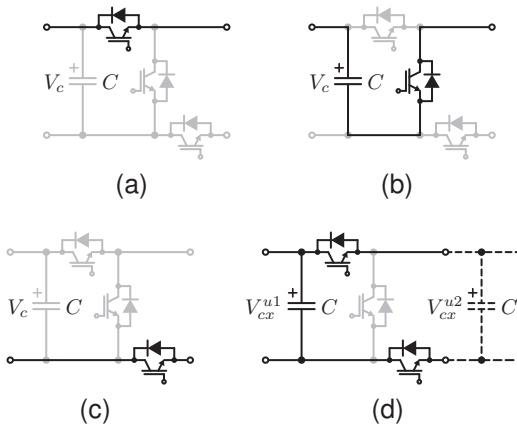


Figure 2. Switching states of the TS module. (a) Positive bypass. (b) Series connection. (c) Negative bypass. (d) Parallel connection.

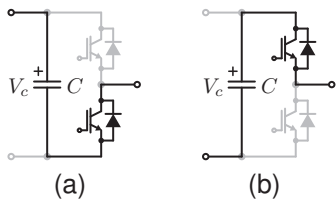


Figure 3. Possible switching states for module connected in the middle point: Series, Bypass.

LVDC (voltages below 1000 Vac and 1500 Vdc as stated in [41], [42]), and at the most these converters can implement solutions up to 6.6 kV [21], [24], leaving an important gap for MVDC applications, as suggested in Fig. 4. The proposed structure can virtually cover the full distribution range besides

an important part of the transmission one, featuring a high-quality integration to ac grids with virtually sinusoidal currents for demanding applications. For example, at LVDC the proposed scheme could compete with the NPCs with balancing leg, as starting from $N = 3$, it would feature a lower device count compared with higher level NPCs, without the issue of asymmetrical blocking voltage. Moreover, the power quality can be enhanced by adding TS cells, hence by steps of three. Then, same structure can also be tailored to further increase the power quality or to interface a MVDC system, by merely adapting the number of modules comprising the strand.

On the other hand, bipolar HVDC systems are typically implemented with two converters (which can be independent LCC or MMC topologies) that control each dc-bus separately, facilitating the asymmetrical load operation. Despite that at this level the changes in the loads are less frequent, transmission links may also suffer from asymmetries in their demand, hence the balancing feature is still required. The structure proposed would be able to implement a bipolar system by splitting a unipolar dc link with the aid of the balancing leg, hence reducing costs and keeping the buses decoupled. This leads to using a single rectifier stage, which can be either MMSPC or MMC based.

Overall, the proposed system allows the operation at both distribution and transmission level, covering from LVDC to HVDC continuously, extending the modularity advantages of the MMC family. Existing solutions at distribution and transmission levels are compared with the proposed system in Tables II and III respectively.

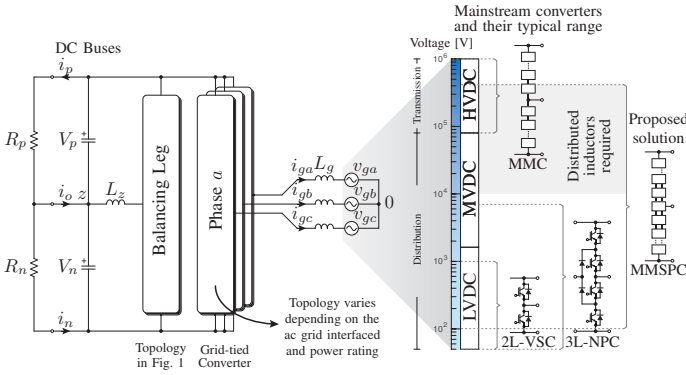


Figure 4. Grid-tied Multilevel Converter with a Balancing Multilevel Leg. Depending on the grid voltage, different topologies or number of cells can be used.

C. Operation Description of proposed Balancing Multilevel Leg

The proposed balancing multilevel leg is connected between the positive and negative poles of the bipolar dc system, while its midpoint is connected to the neutral point of the bipolar system, as it is presented Fig. 4. This connection allows access to both buses in the system, therefore it can redistribute the currents in the bipolar system and suppress the drifting capacitor voltages. The objective is to maintain the dc voltages balanced regardless the load conditions by manipulating the current into the midpoint.

Under symmetrical loading conditions, the power delivered/consumed by the two buses is equal, and there is no current through the midpoint of the dc bus. However, when asymmetries arise, the powers in the two buses are not equal, resulting in non-zero midpoint currents. Furthermore, the two dc-buses can carry the power in opposite directions, allowing one dc-bus is regenerating energy whereas the other one feeding the energy to the loads, which is also reflected in midpoint currents. These processes lead to voltage imbalances at the dc side, and the grid-tied converter does not have enough controllability to correct it. Hence, an external balancing circuit is necessary to maintain the balance regardless the load condition.

In the proposed configuration presented in Fig 4, the operational principle of the balancing leg can be explained following the concept in [13]. Whenever the loads R_p and R_n are balanced, the current flowing at the positive rail i_p coincides with the returning one on the negative side i_n , hence making the current through the neutral conductor virtually zero. This does not hold when imbalances occur, as the non-zero i_0 would alter the dc voltages, and a conventional converter simply cannot regulate this drift. To avoid this issue, the fourth leg is operated to regulate the current flowing through the dc-bus midpoint to keep the dc voltages from drifting. The operational principle of this strategy is to modify the inductor current in such a way that the net current going into the neutral point of the dc-link system is always minimal. This means that, in case of having different loads in the dc-poles, this stage will impose a dc current opposed to the resulting i_0 , in order redistribute the exceeding current and keep the midpoint at V_{dc} . Given

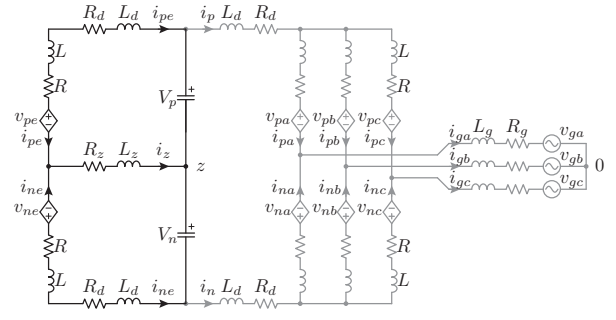


Figure 5. Model of balancing multilevel leg connected to the multilevel grid-tied converter.

that the larger load could be either connected at any bus, this leg should be able to regulate current bidirectionally. Also, as active loads can be present in these systems as well, the principle is also able to balance such scenarios.

III. MODELING AND CONTROL SCHEME

This section will discuss the formulation of the balancing leg model used for designing the regulators. Considering that the grid-tied converter dynamics do not differ substantially from the conventional MMC, the model developed in [43] is adapted to the MMSPC, by using the modulation framework that will be covered in the remainder of the paper.

A. Decoupled-Current Model of Multilevel Balancing Leg

A decoupled-current control model for the balancing multilevel leg can be obtained by extending the analysis in [43]. For this purpose, the model presented in Figure 5 will be employed. Please note that the presence of the balancing leg allows to separate the dynamics from ac and dc sides, hence simplifying the control design tasks. Consequently, there is no loss of generality if the grid-tied converter is a different topology.

To constraint the solution, it is assumed that all modules within the same arm are operated at the same modulation index. Additionally, the capacitor voltage V_c is used as the output voltage quantization, the arm voltages for the balancing converter can be expressed by

$$\mathbf{v}_{xe} = NV_c [m_{pe} \ m_{ne}], \quad (1)$$

where the variables N is the number of TS cells in the strand, m_{pe} and m_{ne} respectively correspond to the modulation indices for the positive and negative arms in the balancing multilevel leg converter.

The modulation indices of this extra leg are composed of two independent components, one being the average or dc component while the other corresponds to the midpoint. This leads to:

$$\mathbf{m}_{xe} = \mathbf{m}_{de} + \mathbf{m}_z \quad (2)$$

where, the vectors \mathbf{m}_{de} and \mathbf{m}_z are defined by:

$$\mathbf{m}_{de} = [m_{de} \ -m_{de}], \ \mathbf{m}_z = [m_z \ m_z] \quad (3)$$

As shown in Figure 5, the dc-link voltage is split into two capacitors, constituting the system's neutral point z . Each pole has its voltage, and ideally $V_p = V_n = V_{dc}$ for a properly balanced dc system. The model is further comprises the converter arm inductance L , the arm losses R , the distribution line parasitics represented by the inductances L_d and resistances R_d . Finally, the neutral conductor dynamics are modeled by a first order system composed of a resistor R_z , accounting for the resistive losses of the inductive filter, and its inductance L_z .

Following the approach presented in [43] along with (1)-(2), it is possible to formulate a decoupled-current control model for balancing a multilevel leg as

$$(L_d + L) \frac{d}{dt} \mathbf{I}_{de} + (R_d + R) \mathbf{I}_{de} = \mathbf{V}_{xe} \mathbf{Q}_1 - N \mathbf{m}_{de} V_c, \quad (4)$$

$$(2L_z + L) \frac{d}{dt} \mathbf{I}_z + (2R_z + R) \mathbf{I}_z = -N \mathbf{m}_z V_c. \quad (5)$$

The vectors \mathbf{I}_{de} , \mathbf{I}_z and \mathbf{V}_{xe} represent the dc current, mid point current and dc input voltage respectively. These vectors are defined as follows:

$$\mathbf{I}_{de} = [i_{pe} \quad i_{ne}]; \quad \mathbf{I}_z = [i_z \quad i_z]; \quad \mathbf{V}_{xe} = [V_p \quad V_n]. \quad (6)$$

We assume that all capacitors are balanced and at their reference voltage level, the dc component of the modulation index \mathbf{m}_{de} can regulate the total dc voltage of the system. Indeed, if all the capacitor voltages of the balancing leg are equal to V_c and a constant modulation index equal to $m_{de} = 0.5$ is set, the total pole-to-pole dc voltage becomes NV_c . By considering the equivalent capacitances of the bipolar system to be equal and the losses of the dc lines similar, it can be assured that both voltages of the bipolar system are equal to $NV_c/2$. This means that the main function of the balancing leg is to act as a dc-dc converter with a constant duty cycle of 0.5 as long as it splits the dc voltage in half. However, if the lines are not equal or there is some mismatch in the bipolar system, it is possible to use this midpoint modulation index (\mathbf{m}_z) as an extra degree of freedom to achieve the balance of the dc voltages in the bipolar system. The aforementioned modulation index regulates the current that flows in the neutral point z and therefore can keep these voltages balanced, regardless of the loads connected to each of the buses. In other words, \mathbf{m}_z maintains the voltages from drifting by providing an additional path for the excess current to return.

B. Control of the Capacitor Modules Voltage

The key control target of the system displayed in Figure 4 is a steady voltage balance of the modules of the balancing multilevel leg and the dc-link. If this control objective is met, the regulation of the dc buses voltages becomes trivial. Therefore, the control scheme objective can be simplified to the following: adjust the ac current flowing into the system in order to guarantee enough energy is being fed to the converter, and then redistribute it accordingly using the modulation stage to keep the cell voltages balanced.

The grid connection control follows a modified version of the voltage oriented control (VOC) scheme [44], as it can be seen in Fig. 6. This cascade control architecture considers an

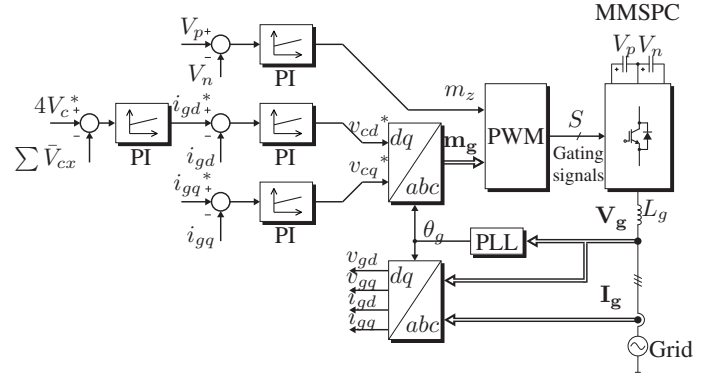


Figure 6. Proposed control loop of the capacitor modules voltage

inner loop that regulates the ac current components in the synchronous dq -reference frame, while the outer loop controls the total stored energy in the system. It is important to consider that the total storage energy in transmission systems including the energy in the modules of the grid-tied converter based on MMC plus the balancing multilevel leg, while in distribution systems this energy is composed by the energy in the dc-link and the balancing multilevel leg.

The inner controllers that regulate the dq components are capable of generating the ac modulation index \mathbf{m}_g to meet the required control objectives. The modulation indices signals are employed in the modulation strategy, which also performs the balancing function (*i.e.*, redistribution of energy among the modules) along with the gating signal generation, as it will be discussed in the following section.

The outer controller is responsible for satisfying the energy demands of the system, which will fully manage the grid integration of the bipolar system. This action is done through the proper adjustment of the d grid current reference. This control loop has some implementation differences for distribution or transmission systems, as displayed in Fig. 6. On the other hand, the reference for the q component of the current is set to an arbitrary value, and for instance, to follow grid requirements such as reactive power compensation or unity-power-factor operation.

C. Balancing of the Bipolar DC System

So far, the control scheme is able to generate a controlled bipolar dc bus and interface the ac grid with adjustable power factor. However, in the presence of different load conditions of the two dc buses, the system requires additional control. The control of asymmetrical load on the dc buses can exploit the extra degree of freedom of the balancing leg, in order to exchange power between the dc buses. This approach controls the middle point dynamically. The model presented in Figure 5 along with Kirchhoff's voltage law entails

$$\Delta V_{dc} = (2L_z + L) \frac{d}{dt} i_z + (2R_z + R) i_z + 2NV_c m_z, \quad (7)$$

where ΔV_{dc} corresponds to the difference between the dc voltages of the system, hence $V_p - V_n$. Using this result, a PI controller is designed. The proposed control loop has also been included in the scheme shown in Fig. 6.

Equation (7) suggests that the midpoint current i_z is a signal with low frequency components. Hence, the balancing leg has to generate this current while maintaining the balance among the capacitor voltages. As mentioned earlier, the parallel connection between the positive and negative arms eliminates second-order power pulsations in the MMSPC with TS modules, allowing the operation of the balancing multilevel leg even under low output frequency. This is done without severe capacitor voltage oscillations at each module. Given that the differences in consumption at the dc side will entail a remanent dc current, this leg should be able to regulate a dc component in order to satisfactorily keep the balance. This would not be possible with a conventional MMC leg, given that the operation at lower frequencies will impose considerable oscillations in the capacitor voltage of the modules.

D. Modulation Framework

The premise of the proposal is that the modulation strategy uses the parallel state for exchanging energy between neighboring modules. Instead of bypassing modules, parallel connectivity is promoted whenever possible. The parallel state will ensure the internal balance of the capacitor voltages among the modules of the same phase, transfer power, and thus enables the correct operation of the system. In this work, the Phase-Shifted Carrier Pulse Width Modulation (PSC-PWM) is employed to the control of the converter [45]. The basic rules for this modulation strategy are presented in Fig. 7 and it can be summarized as follows:

$$\text{state } U_k = \begin{cases} 1 & \text{if } v_u^* \geq C_k \\ 0 & \text{if } v_u^* < C_k \end{cases} \quad (8)$$

$$\text{state } M = \begin{cases} 1 & \text{if } v_u^* \geq C_m \\ 0 & \text{if } v_u^* < C_m \end{cases} \quad (9)$$

$$\text{state } L_k = \begin{cases} 1 & \text{if } v_l^* \geq C_k \\ 0 & \text{if } v_l^* < C_k \end{cases} \quad (10)$$

where $k \in [1, 2, \dots, N - 1]$.

In the previous expressions, the variable U_k corresponds to the switching signal for the k -th upper arm module, L_k is for the k -th lower arm module, and M is for the half-bridge cell connected to the midpoint. The variables C_k and C_m ($\in [0, 1]$) are the phase shifted carriers while v_u^* and v_l^* are the total modulation indices for the upper and lower modules respectively.

Under this modulation scheme, the states 0 and 1 correspond to parallel and series connection for the modules driven by the signals U_k and L_k (Fig. 2). Then, for the module connected in the middle of the strand, the states 0 and 1 means bypass and series connection respectively (Fig. 3). The repeated use of the parallel states significantly simplifies the balancing of the cells, which along simplifies its implementation and required sensing.

By properly using the additional states featured by the MMSPC through the modulation, a sensorless approach to keep the voltages balanced is enabled. Also, in this way additional control loops are avoided, greatly simplifying the control complexity [31]. This is not possible with traditional

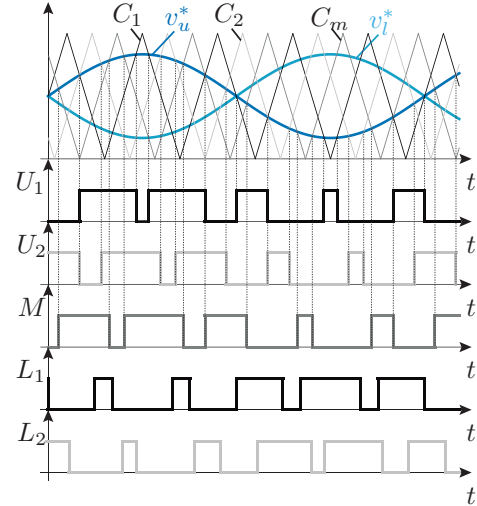


Figure 7. Phase-shifted modulation scheme for the MMSPC.

modules in the conventional MMC, such as half or full bridges, given that these structures feature only series and bypass states. Under this scenario, to achieve the internal voltage balance of all the modules connected in the system, it is necessary to control the charge-balancing current for each module via dedicated control loops, which have to be in accordance with a modulation strategy [25]. Consequently, these approaches require sensing the cell voltages of the entire system.

As discussed earlier, the MMSPC enables an extra power-transfer route through the parallelization of the cells, which cancels the voltage imbalances among the modules [28], [46]. Indeed, the parallel connection between the modules creates equalization currents to clear the voltage differences [32].

However, since the equalization current emerges spontaneously to keep the module voltages balanced during the parallel connection, it is important to consider that this method imposes a trade-off between the switching frequency, module capacitance, and the magnitude of the equalization currents, as suggested by [31].

E. Design Considerations

The possibility of the parallel interconnection brings substantial benefits to the overall performance of the converter, mainly a great simplification in the energy redistribution within the MMSPC. However, it is important to mention that some thought has to be put into the overall design in order to avoid incurring in excessive losses, or more importantly safety concerns. The parallel connection of capacitive sources can lead to current spikes if the voltage difference between the cells being connected is large enough and there is no impedance between them to suppress it. These currents can be addressed in several ways. First, voltage differences build up during switching periods without parallelization or alternative balancing activities. As in conventional MMC, the faster the system can adjust states to balance capacitors or to clear differences through parallelization, the lower the maximum voltage differences between them, decreasing the energy that drives current surges and is proportional to the squared voltage

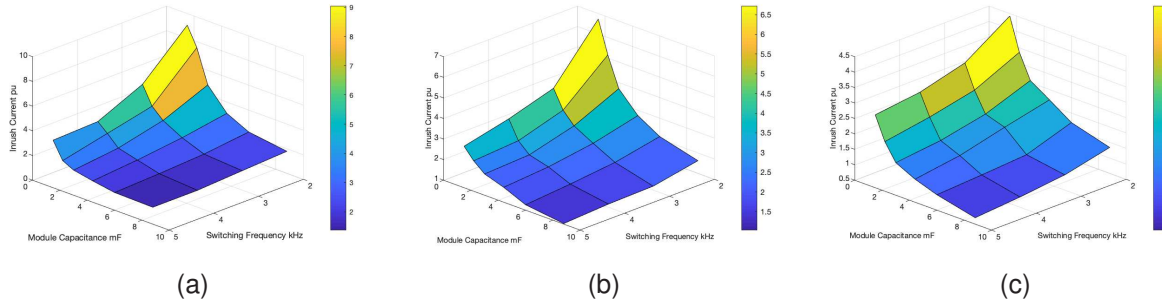


Figure 8. Normalized inrush current during parallelization for different switching frequency and capacitance values. (a) 50 nH stray inductance. (b) 200 nH stray inductance. (c) 800 nH stray and distributed arm inductance.

differences. Thus, a high switching frequency could be used, in order to ensure the voltages are always tightly regulated, and giving no room for large voltage mismatches, but at the cost of higher switching loss depending on the converter power rating. In addition, the capacitance mitigates the build-up of voltage differences and consequently surge currents. Third and most importantly, the impedance through given by the semiconductor switches and the module interconnection to the next module's capacitor limits the current. Foremost, the inductive part of the impedance restricts the current derivative and determines the equilibration speed together with the capacitance.

On a different perspective, and considering the functionality and features of the TS cell, the same analysis for losses and current spike suppression performed in [29], [31] can be applied. It balances the capacitance, switching frequency and additional impedance to achieve a trade-off between the energy dissipated in the parallelization of the cells and the resulting conduction losses, or in other words, modify the damping of the equivalent damped resonant circuit through a proper circuit design. First, regarding the capacitance value, a common criteria for sizing the cells in a modular converter is based on inertia requirements that meet the energy balance of the converter. According to [47], [48], a modular converter should have 30 to 40 kJ/MVA, which would lead to a capacitor voltage ripple in the 10% range with a moderate capacitance. Finally, assuming the requirements in capacitance along a moderate switching frequency, the additional impedance needed to effectively suppress current spikes to an acceptable value is greatly reduced. Moreover, the parasitic elements in the parallel path would be enough to reduce these spikes: this path is made through two turned-on switching devices, which accounts for a resistance of 5 to 20 $m\Omega$ depending if IGBTs or MOSFETs are being used [49], [50]. Furthermore, the latter are typically packaged in modules that provide an average stray inductance in their leads 15 nH [49], [51], [52], which is to be added to the inductance of the connecting wires, which for a 200 A interconnection with length 10 cm and a spacing between the individual conductors of the pair of 5 cm would increase the path inductance in about 80 nH [53].

Thus, already a fairly moderate sizing on the reactive components eliminates large spikes of current during parallelization, and in most cases does not even require additional

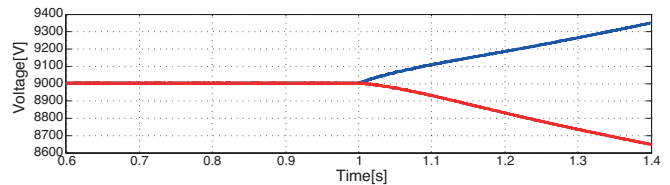


Figure 9. DC-Bus voltages from a bipolar system based only in a three-phase grid-tied multilevel converter.

Table IV
SIMULATION PARAMETERS

Parameter	Value
Module capacitance (balancing multilevel leg) C	2.2 mF
Number of modules per arm (balancing multilevel leg) N	6
DC-Bus voltages V_p, V_n	9000 V
Grid inductance L_g (with multilevel grid-tied converter)	10 mH
Bipolar dc-bus capacitance C_{dcx}	5 mF
Bipolar dc-bus load resistance R_{dcx}	500 Ω
Midpoint inductance L_z	15 mH
Arm Inductance L	15 mH

components. This can be observed in Fig. 8, where the dependence of the normalized inrush current is studied in terms of different capacitance and switching frequency values. The study considered three cases, varying the port inductance considered in the parallel path: 50, 200 and 800 nH, and the spikes were normalized with respect to the output current. As stated earlier, the first two cases are virtually covered in terms of parasitic inductance, while the latter one considers these stray values and additional port inductors by distributing the arm inductance. Results indicate that given the proper trade-off between capacitance and switching frequency, an inrush current within the devices ratings can be achieved in all three scenarios (typically 2 to 3 times the rated current), using moderately sized capacitors and adequate switching frequencies for high-power applications.

IV. SIMULATION RESULTS

Before demonstrating the overall performance of the proposal, Figure 9 shows the simulation of the dc-bus voltages of a bipolar system without a balancing mechanism. Given that this approach only regulates the total dc-link voltage, the bus voltages will be only balanced when the loads are symmetrical.

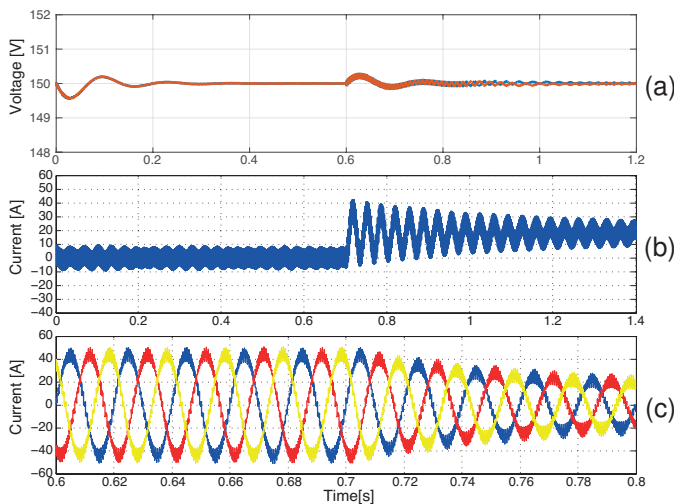


Figure 10. Dynamics of the bipolar system. (a) dc-link voltages (b) Mid point current (c) Grid currents.

Initially both dc-buses are balanced, hence the bipolar bus operates normally. However, in $t = 1$ [s], the passive load is disconnected from the upper bus, while a rated load is kept connected to the lower dc-bus. In this moment the bipolar dc system enters into an asymmetrical operation and, as it can be seen in Figure 9, the dc-bus voltages start to diverge. Given that the grid-connected converter does not have the capability of redistributing the currents using the neutral conductor, this condition cannot be corrected. The system needs additional circuitry to be able to guarantee balanced operation under any load scenario. The simulation parameters for a MV system are provided in Table IV. It is important to highlight the fact that this asymmetrical operation will generate unbalanced dc voltages in the bipolar system, regardless of the system parameters values.

The same parameters in Table IV are used to implement a simulation model to validate the proposed system and the balancing mechanism. This considers a load impact in the positive dc-bus, in order to switch from a symmetrical operation to an asymmetrical one, demonstrating the capability of the proposed system to maintain the balance of the buses in both scenarios. The grid-tied converter is a three-phase multilevel system, where each phase of the system is based on the proposed topology presented in Fig. 1. In addition, a balancing leg based on the same topology is added to handle dc-side asymmetries. The load impact takes place at $t = 0.7$ [s], when the passive load is disconnected from the upper bus, while a the load connected to the lower one remains unchanged.

Figure 10 shows the dc voltages of the bipolar system, the current flowing through the midpoint (I_z) and the grid currents. It can be seen that in Fig. 10a the bipolar system remains balanced in both symmetrical and asymmetrical load operations, unlike the case presented in Figure 9, where the voltages of the dc-buses began immediately to diverge when the asymmetry arose. Instead, the proposed bipolar system maintains both dc buses balanced to 9000 V, both in symmetrical or asymmetrical operation. As previously mentioned, the key to achieving balanced operation of the system is the dc

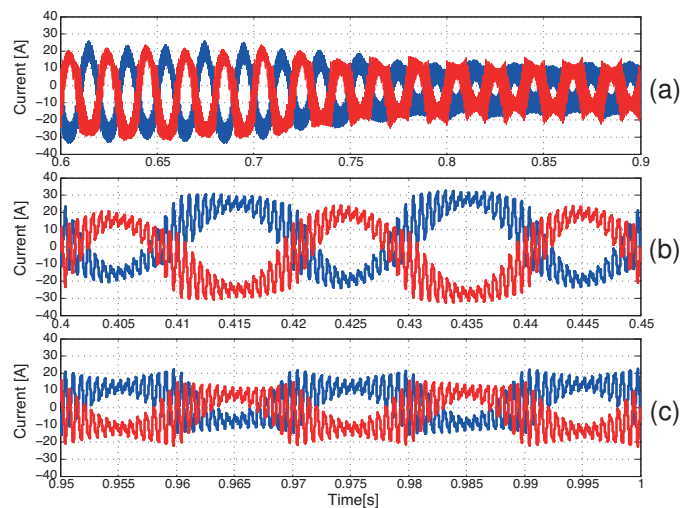


Figure 11. Dynamics of the arm currents of the Grid-tied converter. (a) Arm currents during the whole test. (b) Arm currents in symmetrical operation. (c) Arm currents in asymmetrical operation.

currents redistribution in such a way that the midpoint current is virtually zero. By achieving this condition, the voltage difference will be cancelled allowing the system to operate continuously. This operation becomes clear in Fig. 10b. This figure shows the balancing current I_z . When the system is operating in a symmetrical condition, there is no need for compensation, and the net current flowing through the balancing leg equals zero. However, when the imbalance occurs in the loads of the dc link, the non-zero current flowing through this balancing leg allows minimizing the net current going into the midpoint. This compensation maintains the voltages at the same value and balanced. Please note the nature of i_z , by being a dc quantity the regulation of this current with a conventional MMC balancing leg is not feasible, given that the low-frequency oscillations at the cells would turn the system unstable. The MMSPC, however, regulates this current and does not alter the voltage distribution in the cells.

On the other hand, Fig. 10c shows the grid currents (i_{ga} , i_{gb} , i_{gc}). The grid currents' waveforms are directly linked to the grid-tied converter topology. As this simulation uses a multilevel converter, the waveform of this current has low THD. However, as mentioned above, the proposed bipolar scheme is compatible with any grid-tied converter topology. From Fig. 10c, it is possible to identify the moment when the dc load is disconnected, the grid currents are reduced accordingly in order to achieve the total energy balance of the system.

Figure 11a displays the positive and negative arm currents of one phase of the grid-tied converter. As it can be seen in these figures, the arm currents maintain the balance in either symmetrical (Fig. 11b) and asymmetrical (Fig. 11c) operation modes. When the asymmetrical operation takes place, the current flowing through the arm is reduced, because only one dc-bus is feeding a load.

The capacitor voltage waveforms of phases a and b of the grid-tied MMSPC, besides the ones from the multilevel balancing leg are shown in Fig 12. The voltage in the modules

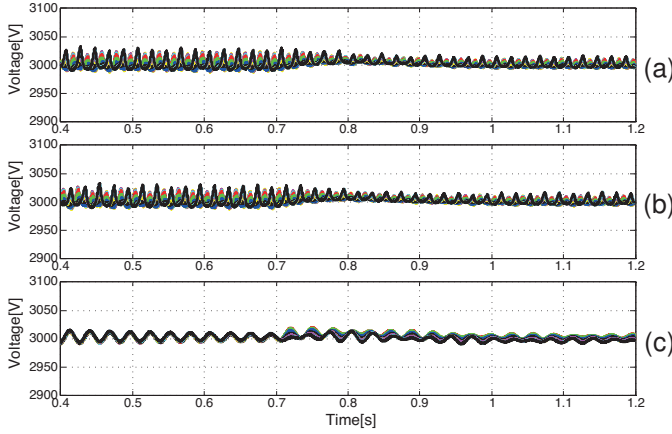


Figure 12. Dynamic response of the module voltages. (a) Voltage of modules connected in the phase A (b) Voltage of modules connected in the phase B (c) Voltage of modules connected in the multilevel balancing leg.

of the grid-tied converter are presented in Fig. 12a and Fig. 12b. It is clear that the balancing strategy achieves the objective, keeping the system balanced either in balanced and unbalanced scenarios. In order to not overextend this analysis, the dynamics of phase c are not presented, but it is understood that the dynamics presented are replicated in phase c . Regarding the balancing leg, Fig.12c provides the dynamics of the cell voltages forming it. The voltages in these modules present a similar dynamic response that the grid side modules, confirming the correct operation of the balancing strategy implemented in the modulation stage. Again, this balance is obtained with the parallel connection strategy between adjacent modules implemented in the modulation scheme, and therefore, it does not require voltage/current sensing for achieving the internal balance of the whole system.

Additionally, Fig.13 presents the center module voltages for the aforementioned legs of the system. It can be seen in Figures 13a, 13b and 13c, that the voltages in these modules exhibit similar dynamics than the rest of the arm modules, showing again the effectiveness of the proposed balancing mechanism.

To complete the analysis, Fig. 14 present the arm and load voltages of the grid-tied converter. As mentioned above, in this simulation a multilevel grid-tied converter is used. The number of modules per arm is $N = 6$, and it can be seen in Figures 14a and 14b that each arm is able to generate 7 positive voltage levels. Note how the capacitor voltage V_c is the voltage quantization in the synthesized waveform. Finally, the phase voltage generated by the grid-tied converter is shown in Fig.14c, where the same seven levels appear, but with positive and negative polarity, hence allowing interconnection with the ac grid.

V. EXPERIMENTAL VALIDATION

The proposed system is tested in a scaled-down experimental prototype, which is shown in Figure 15. The implemented system is based on the structure of Fig. 4, so it considers a grid-tied converter based on a 3-phase 2L-VSC topology plus the balancing MMSPC leg, whose parameters are presented in

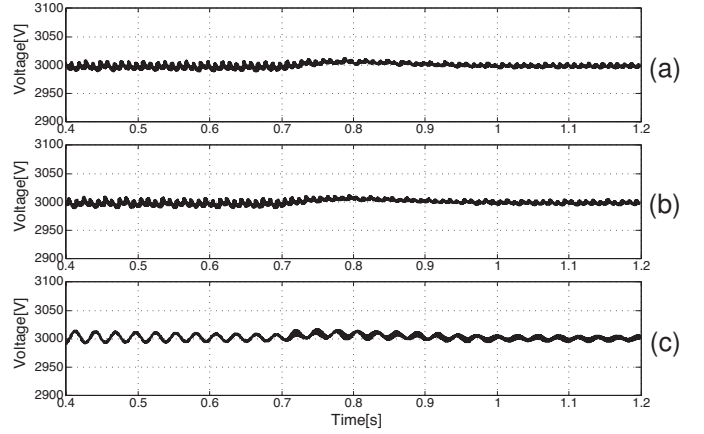


Figure 13. Dynamic response of the center module voltages. (a) Voltage of module connected in the center of phase a V_{ca}^m (b) Voltage of module connected in the center of phase b V_{cb}^m (c) Voltage of module connected in the center of balancing leg V_{ce}^m .

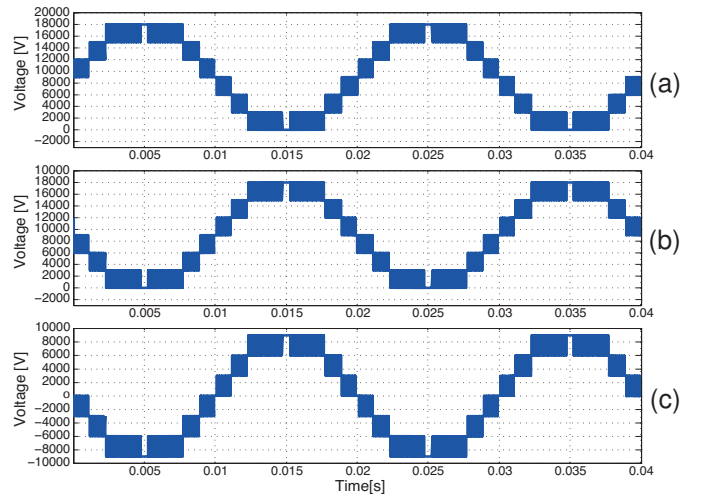


Figure 14. Dynamic of the arm and load voltages of the grid-tied converter. (a) Voltage of the positive arm v_{pa} . (b) Voltage of the negative arm v_{na} . (c) voltage generated by the grid-tied converter.

Table V
EXPERIMENTAL PARAMETERS

Parameter	Value
Module capacitance (balancing multilevel leg) C	0.5 mF
Number of modules per arm (balancing multilevel leg) N	3
DC-Bus voltages V_p, V_n	80 V
Grid inductance L_g (with 2L-VSC)	10 mH
Grid inductance L_g (with multilevel grid-tied converter)	5 mH
AC frequency	50 Hz
Bipolar dc-bus capacitance C_{dcx}	0.5 mF
Bipolar dc-bus load resistance R_{dcx}	50 Ω
Midpoint inductance L_z	10 mH
Arm Inductance L	5 mH

Table V. The purpose of implementing the grid-tied converter with a 2L-VSC topology is precisely to highlight the versatility of the proposed dc-bipolar system, extending its application to any grid-tied system enabling a unipolar dc bus, and turning it into a bipolar one with the aid of the balancing leg. A microLabBox-dSPACE serves as a programmable control plat-

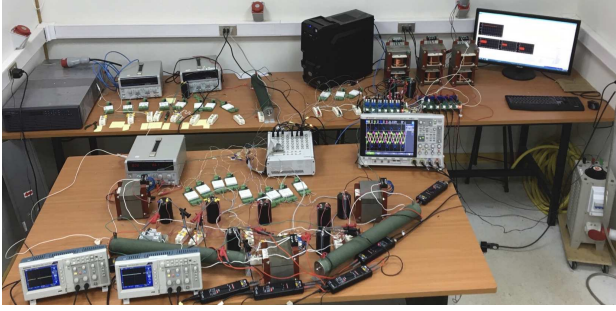


Figure 15. Experimental setup of the Grid-tied 2L-VSC converter with a balancing multilevel leg.

form. To fully validate the features of the promoted structure, a second set of results is obtained using a single-phase MMSPC rectifier with the corresponding balancing leg, in order to highlight the possibility of using the proposed structure as a power electronics building block, and extend its modularity to any voltage level.

A. Dynamic response with 2L-VSC grid interface

For the experimental validation of the proposed scheme, the system will intentionally driven to an asymmetrical operation. For this evaluation, a sudden load drop takes place in one of the buses while the other one remains with the nominal load. Figure 16a provides the dynamic performance of the bipolar dc system in the aforementioned scenario. It can be seen how the evolution of the dc bus voltages is similar, as the load tends to disturb the voltage, which the controller compensates by adjusting the input current amplitude, and the system returns to normality. This situation is displayed in Fig. 16ai. The

reason for this behavior is the regulation of the midpoint current provided by the additional leg. Figure 16a(ii) presents the response of the capacitor module voltages, confirming the satisfactory performance of the balancing approach proposed. In order to validate the balancing of the converter, Fig. 16a(iii) shows the voltages of two modules of the converter: one belonging to the upper arm V_{ca}^{u1} and one from the lower arm V_{ca}^{l1} of the balancing leg.

Similarly, the system is driven to the reverse scenario, and its response on the dc side is presented in Fig. 16b. The displayed waveforms demonstrate how the system is also able to compensate the asymmetry enforced in the loads, exhibiting a similar performance as in the previous case. As expected, the system is able to overcome both scenarios, maintaining constant dc voltages and thus enabling the use of the MMSPC in bipolar dc applications.

Following with the experimental study, both tests have shown similar responses to the sudden load changes. These load changes have the same effect on the ac side given that the same total power is demanded in both scenarios; therefore only a single set of waveforms will be presented for the grid side quantities. Figure 17 shows the evolution of the grid voltage and current. From the displayed response, it can be seen how the system suddenly decreases its power demand at the moment the loads are disconnected, which is reflected in a controlled decrease of the grid current amplitude performed by the VOC loop. Also, the grid feeds power to the dc system and the controller intentionally enforces unity power factor.

Finally, the balancing current i_z is presented in Fig.18, which validates the operation of the system under both symmetrical and asymmetrical conditions. The capability of redistributing the current when imbalances are present is key

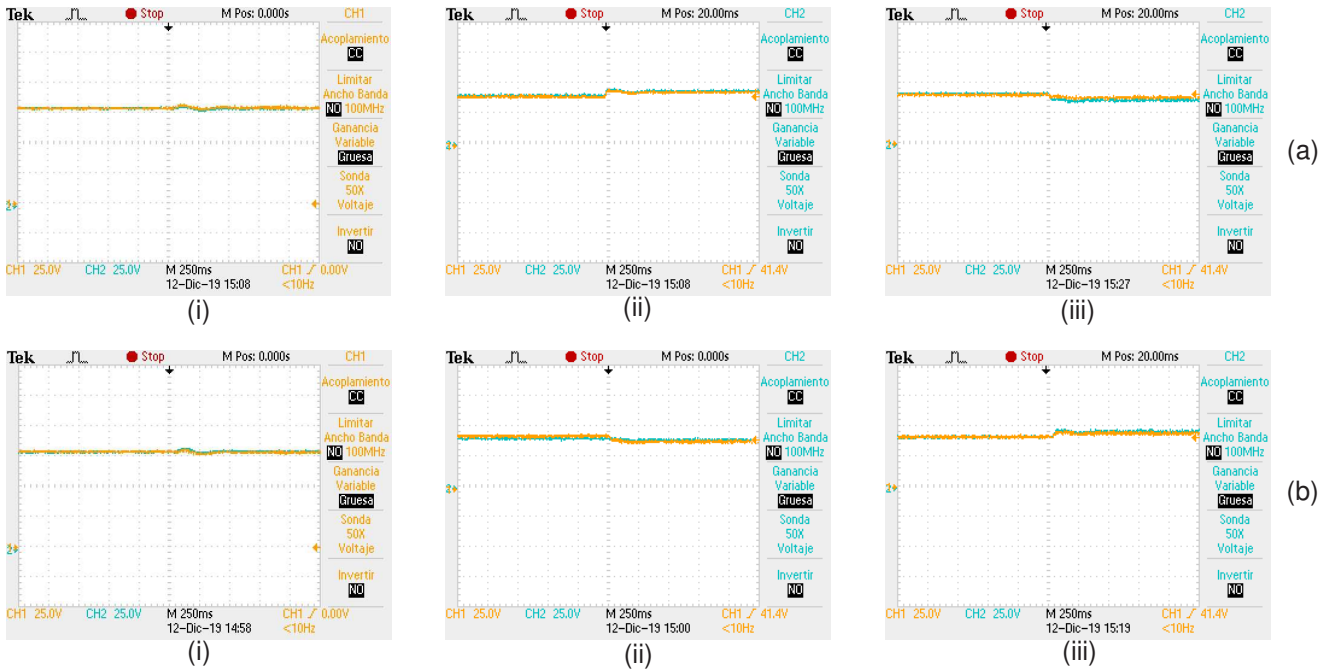


Figure 16. Dynamic response of the dc voltages under asymmetrical scenarios: (a) Upper dc bus unloaded. (b) Lower dc bus unloaded. (i) Ch1 upper dc voltage V_p (25V/div) ; Ch2 lower dc voltage V_n (25V/div); (ii) Ch1 upper arm module voltage V_{ce}^{u1} ; Ch2 upper arm module voltage V_{ce}^{u2} ; (iii) Ch1 lower arm module voltage V_{ce}^{l1} ; Ch2 lower arm module voltage V_{ce}^{l2} .

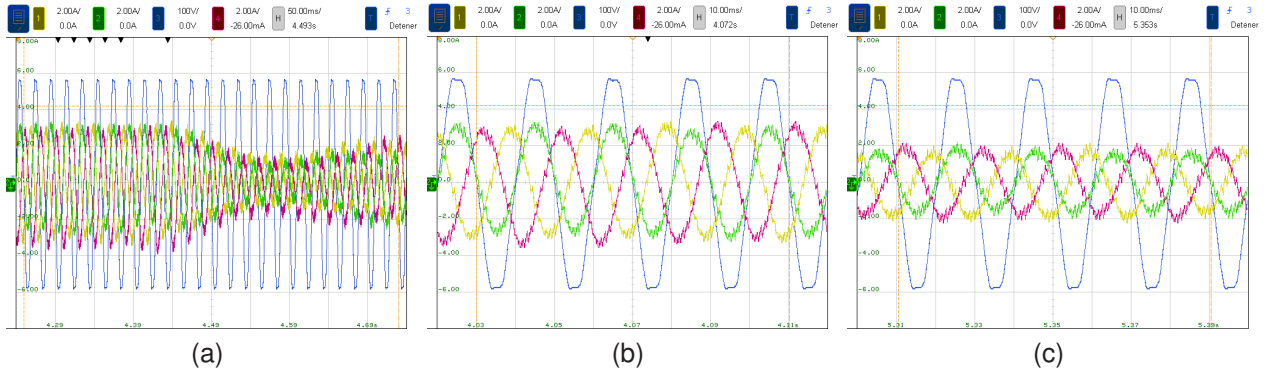


Figure 17. Dynamic response of the ac side under asymmetrical loads. Ch1 grid current i_{gC} (2A/div); Ch2 grid current i_{gA} (2A/div); Ch3 grid voltage v_{gA} (100V/div); Ch4 grid current i_{gB} (2A/div). (a) Dynamic performance. (b) Steady-state operation before impact. (c) Steady-state operation after impact.

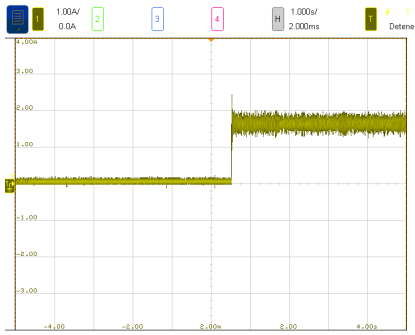


Figure 18. Dynamic response of the middle point current Ch1 i_z (1A/div).

to keep the bipolar system voltages balanced. When the system is operating symmetrically, there is no need for compensation; hence, the current i_z is equal to zero. However, when the demand is not balanced, the current i_z takes the value of the load current in order to redistribute the current in the dc-link stage and cancel the net current through the midpoint to avoid any voltage asymmetries. From Fig. 18, it is clear that i_z waveform is dc nature, which forces the proposed balancing multilevel leg to not be a traditional MMC topology.

B. Performance under regenerating mode with 2L-VSC grid interface

In order to fully validate the features of the proposed system, an active load is connected to the system. This load consists of an external dc power supply of 190 V and a series resistor. This active load is suddenly connected to the lower dc bus while the upper dc bus feeds a simple resistive load. Figure 19 shows the results and confirms that the system is able to handle any load condition and maintain its stability. The evolution of the dc voltages displayed in Fig. 19a demonstrates the performance of the topology and stable operation of the proposed control scheme. The sudden connection of the active load increases the voltages due to the excess energy in the system. However, the VOC loop acts quickly and adjusts the ac input currents accordingly to stabilize dc voltages. The same effect can be seen for the module voltages in Fig. 19b.

The outer voltage loop keeps the module voltages controlled at their reference as it adjusts the ac current amplitude to

achieve that control objective. This behaviour is explained by Fig. 19, where the corresponding changes in i_{gA} magnitude and phase are clear. To compensate the disturbance in the dc voltages caused by the sudden power inflow from the dc side, the control strategy reduces the ac current, which—considering the difference in the power demanded and received—results in the reversal of the ac power flow. In other words, in steady-state with connected dc source, the ac voltage and current waveforms are in phase as the dc system feeds energy into the ac grid.

C. Performance with a single-phase MMSPC rectifier and balancing leg

To complete the experimental studies, a set of single-phase results has been included in order to show the versatility of the proposed topology. In the following tests, two legs of the MMSPC structure of Fig. 1 are being employed, one interfaces the ac grid while the other performs the regulation of the bipolar network. Figure 20 displays the obtained results when repeating the same passive load imbalance scenario in previous sections. It can be seen how the use of a multilevel leg leads to higher input current quality, thereby highlights the lower filtering requirements of the proposed structure. As explained earlier, the modulation stage is able to maintain the inner balance among the cells, and validate the capabilities of the converter. The proper energy distribution along the cells, besides the dc current handling by the balancing leg allows a stable operation at the ac side. It can be seen how the proposed MMSPC features input currents that are practically sinusoidal without employing large input filters, hence enabling its use in high performance and demanding applications.

VI. CONCLUSION

This paper presented a bipolar-type dc system based on a topology inspired by the modular multilevel series/parallel converter (MMSPC). The proposed converter features the usage of a module structure with three switching devices, and this module topology can dynamically interconnect the modules in either series or parallel. The parallel connection allows eliminating the cell voltage oscillations for lower output frequencies so that the proposed structure can handle dc

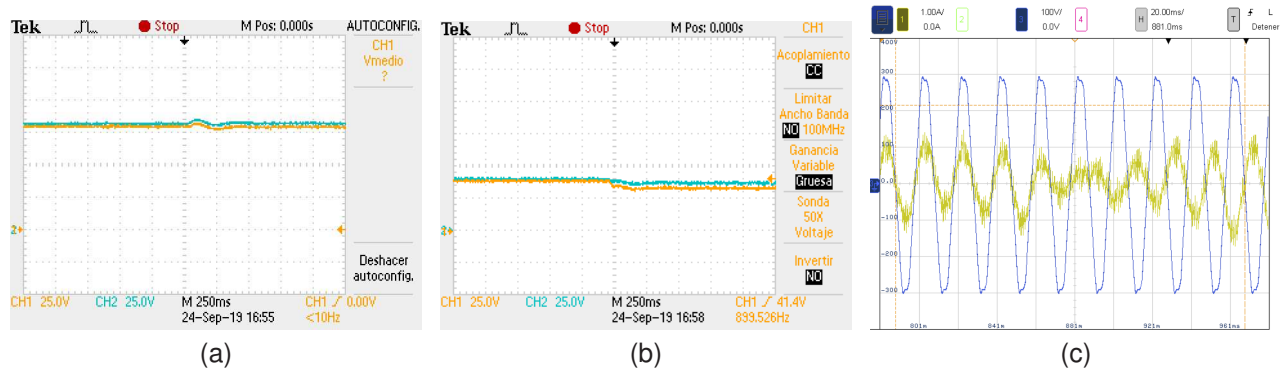


Figure 19. Dynamic response of the system under power reversal. (a) DC bus voltages: Ch1 upper dc voltage V_p (25V/div); Ch2 lower dc voltage V_n (25V/div). (b) Module voltages: Ch1 upper arm module voltage V_{ce}^{u1} ; Ch2 lower arm module voltage V_{ce}^{l1} . (c) Grid-side quantities: Ch1 grid current i_{ga} (1A/div); Ch3 grid voltage v_{ga} (100V/div).

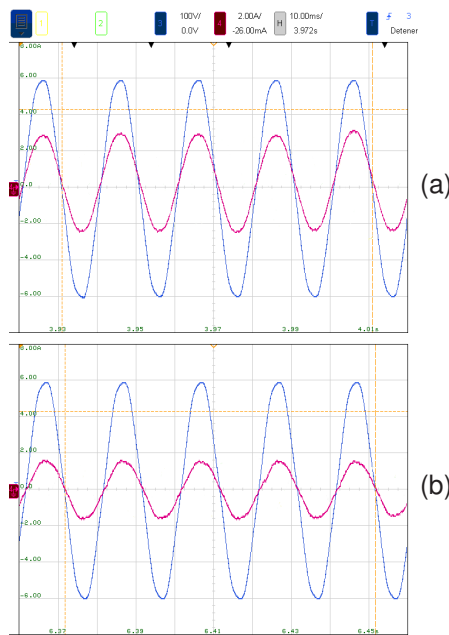


Figure 20. Steady-state response of the single-phase MMSPC under asymmetrical loads. Ch3 voltage v_{ga} (100V/div); Ch4 grid current i_{ga} (2A/div). (a) Steady-state operation before impact. (b) Steady-state operation after impact.

quantities. Due to the modular structure of the MMSPC, adding or removing modules in each arm can set the operation voltage of the system to practically any level. This means that maintaining the same operational principle and complexity, the solution is suitable for both LV-, MV- and HVDC bipolar grids. The paper further introduced a decoupled control and modulation strategy, which enables the use of the parallel connection among the modules of the positive and negative arms of the converter for achieving stable operation of the dc grid, regardless of the load condition of the buses. The proposed system is also easier to control, because the parallel power-transfer channel obviates closed-loop controls in inter- and intra-arm balancing; hence, only the modulation covers this tasks. The guaranteed balance allows exploitation of the high performance offered by the MMC family also in low-frequency and dc applications. The proposed bipolar system

and control strategy were evaluated under asymmetrical load conditions with both power-flow directions. In all modes, the controller achieved stable and good performance, which demonstrates the feasibility of the proposed bipolar systems for low and high voltage applications.

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