A Reduced Series/Parallel Module for Cascade Multilevel Static Compensators Supporting Sensorless Balancing

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***Abstract*—Cascaded multilevel converters have been gaining popularity in static compensators (STATCOMs) owing to their excellent modularity, output quality, and fault tolerance. However, cascaded multilevel converters require a large number of galvanically isolated voltage sensors and complex communication systems in order to balance the module dc-link voltages.**

This paper proposes a reduced series/parallel module (RSPM) that intends to replace H-bridges in cascaded multilevel STATCOMs. Any adjacent RSPMs can be configured in series, bypass, or parallel. Cycling the parallel state through all modules balances all capacitor voltages in a sensorless manner. Since the RSPM-balancing process occurs at the hardware level, H-bridges can be easily replaced by RSPMs without changing higher-level control loops. Compared to existing series/parallel modules, the RSPM has the same functionalities but uses 25% fewer transistors. Despite the reduced switch count, the RSPM is shown to achieve even better efficiency under certain load conditions. The RSPM also attains similar semiconductor utilization ratio as H-bridge modules. The features of the RSPMs are verified on simulations and a down-scaled experimental setup.

***Index Terms*—Static compensator; modular multilevel converter; series/parallel module; sensorless module balancing.**

GLOSSARY OF TERMS

N	Number of modules per arm.
k	Numbering of the modules, $k = 1, 2, \ldots, N$.
n_{out}	Number of inserted modules per arm, $-N \le n_{\text{out}} \le N$.
C	Module capacitance.
L_{diff}	Inductance along the balancing path.
L'	Effective inductance along the balancing path.
f_{sw}	Switching frequency at each module.
ω	The grid angular frequency.
v_{arm}	Arm output voltage.
v_k	The kth capacitor voltage.
$\mathbf{v}$	Vectorization of v_k over all k's.
$i_{k-1,k}$	Balancing current between $k-1$th and kth modules.
i_{arm}	Arm output current.
i_k	The effective load seen by the kth capacitor.
$\mathbf{i}$	Vectorization of i_k over all k's.
r_1	On-state resistance of the up and bottom transistors.
r_2	On-state resistance of the middle transistor.
r	Total resistance along the balancing path.
r'	Effective resistance along the balancing path.
m	Instantaneous modulation index.
M	The peak modulation index over the sin-period.
$\mathbf{x}$	The state of the dynamic system, $\mathbf{x} = [\mathbf{v}^{\text{T}}, \mathbf{i}^{\text{T}}]^{\text{T}}$.
λ	Eigenvalue of the system equation.
x_λ	Eigenvector with eigenvalue of λ.

I. INTRODUCTION

A. Background

STATIC Compensators (STACOMs) are instrumental for ac transmission and distribution systems [1]–[6]. In STATCOMs, the cascade multilevel structure—backboned by cascaded H-bridges (CHBs)—is particularly popular due to its excellent modularity, scalability, output quality, and fault tolerance [7]–[9].

Stable operation of cascade multilevel STATCOMs crucially depends on the balance of individual dc-link capacitors, which is achieved by modifying the carriers or references [10], [11], sort-plus-selection methods [12], as well as direct vector computation [9], [13], [14]. However, since most cascaded multilevel structures implement H-bridges, all balancing methods require isolated voltage sensors and data-transmission systems, which increase the system cost and complexity [15].

B. Prior Work on Hardware-level Balancing

Apart from improving the existing algorithms for balancing, alternative circuit topologies have been explored to shift the balancing efforts to the hardware level. Reference [16] extends the H-bridge modules with additional diodes, inductors, and transistors so that the modules can be paralleled in pre-defined pairs. The drawbacks, however, include large component count and limited scalability. The additional transistors are in series with the inductors, likely encountering large overshooting voltage during turn-offs. Voltage sensors are still mandatory since the parallelization does not extend across pre-defined module pairs. Reference [17] packs every two H-bridge modules into one unit. Similar to [16], such a composite module can parallelize two internal capacitors. The methods in [16], [17] share the idea of using hardware parallelization to offset the monitoring and communication effort; however, neither extends the parallelization beyond pre-defined module groups, and each module group still requires voltage measurement. The sensory and communication complexity still roughly scales with the module count.

Along the idea of hardware-level balancing, [18] proposed a module that affords fully scalable series/parallel connectivity. Conceptually, the series/parallel module (SPM) splits each H-bridge transistor into two independently-controlled transistors,

each with halved current rating. The doubled transistors and two interconnection wires allow parallelization between any adjacent modules. Since the parallel configuration does not contribute to the arm output voltage, existing modulation strategies use it to replace the bypass to achieve sensorless balancing at the hardware level. Other benefits of SPM include load sharing and thus decreased conduction losses [19], [20]. Compared to [16] and [17], the SPM achieves a completely autonomous balancing. Compared to H-bridges, the SPM maintains the same semiconductor utilization ratio, but doubles the number of independent transistors.

C. Contribution

This paper presents a reduced series/parallel module (RSPM) based on the original SPM [18]. The RSPM obviates two transistors compared to [18] but retains the autonomous balancing feature. For purely reactive loads (i.e., STATCOMs), we find the optimal distribution of the transistor on-state resistance so that the RSPM achieves a similar semiconductor utilization ratio as the SPM predecessor and the H-bridge. Based on the proposed modulation scheme, we provide an analytical model of the module balancing process. The model proves the balancing stability and its independence from other control loops, which are also verified by simulations and experiments. These features allow an easy upgrade from CHBs to RSPMs without changing the upper-level controls.

This paper is organized as follows. Section II introduces the RSPM topology and derives an equivalent circuit model for further analysis of the balancing mechanisms. Section III analyzes the balancing dynamics and compares the losses with existing modules. Section IV presents experiment results, and Section V concludes the paper.

II. Topology and Operating Principle

A. Basic Topology and Switching States

Fig. 1(a) shows a cascaded multilevel STATCOM featuring the proposed reduced series/parallel module (RSPM). The RSPMs can be configured as series, bypass, and parallel states [Fig. 1(b)]. Fig. 1(c) compares a RSPM to a cascaded H-bridge (CHB) (N = 4) under different configurations. In the example of n_{out} = 2, the RSPM connects two pairs of modules in series; each pair applies a parallel state to ensure balance within. Balancing across the pairs can be achieved in another switching cycle that assigns a parallel mode in the middle. Since the parallel state does not alter the output voltage, we use it instead of bypass in the scheduling scheme. Specifically, given the required output level n_{out}, the scheduler assigns $|n_{\text{out}}|$ series states and fills the rest with the parallel state. Cycling the series states through the arm ensures equal parallel opportunity at each switching site and thus the balance of the entire arm. Within this setting, RSPMs always involve all modules regardless of the output, whereas the CHB must bypass some modules when $|n_{\text{out}}| < N$.

Since the parallel state is jointly determined by two adjacent RSPMs, we partition the RSPM string into $N-1$ switching sites (labeled as L_k, k = 1, …, $N-1$), each covers an interconnection part. To simplify the discussion, we lump the remaining six transistors (labeled as L_{N+} and L_{N-}) near the arm's terminals as the terminal switching site, L_N. The two middle switches at L_{N+} and L_{N-} can be omitted in implementation.

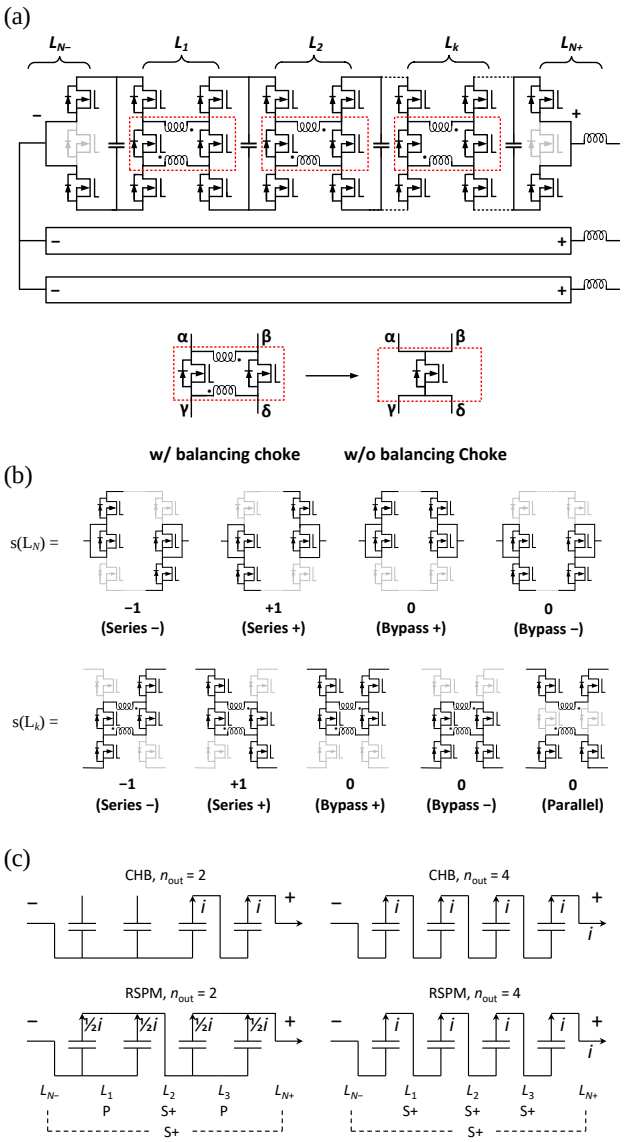


Fig. 1. (a) The cascaded multilevel STATCOM featuring the proposed reduced series/parallel module (RSPM). (b) The RSPM switching states. (c) Simplified CHB and RSPM diagrams at comparable output levels.

We define the switching states for L_1–L_N as in Fig. 1(b). All N switching sites modify the arm output voltage in an independent, additive manner according to

$$v_{\text{arm}} = \sum_{k=1}^{N} s(L_k) V_{\text{dc}}, \tag{1}$$

where $s(\cdot)$ denotes output voltage level of the switching state, V_{dc} the module voltage assuming balance, and v_{arm} the arm output voltage. Similar to cascaded H-bridges, $-NV_{\text{dc}} \le v_{\text{arm}} \le NV_{\text{dc}}$. Here, we use k (= 1, …, N) to enumerate the switching sites.

In summary, the RSPM behaves identically to CHBs with respect to the output voltage quantization but lowers the current stress on the capacitors and provides intrinsic module balancing. These merits allow the RSPM to directly replace CHBs without altering the arm-level control. The balancing

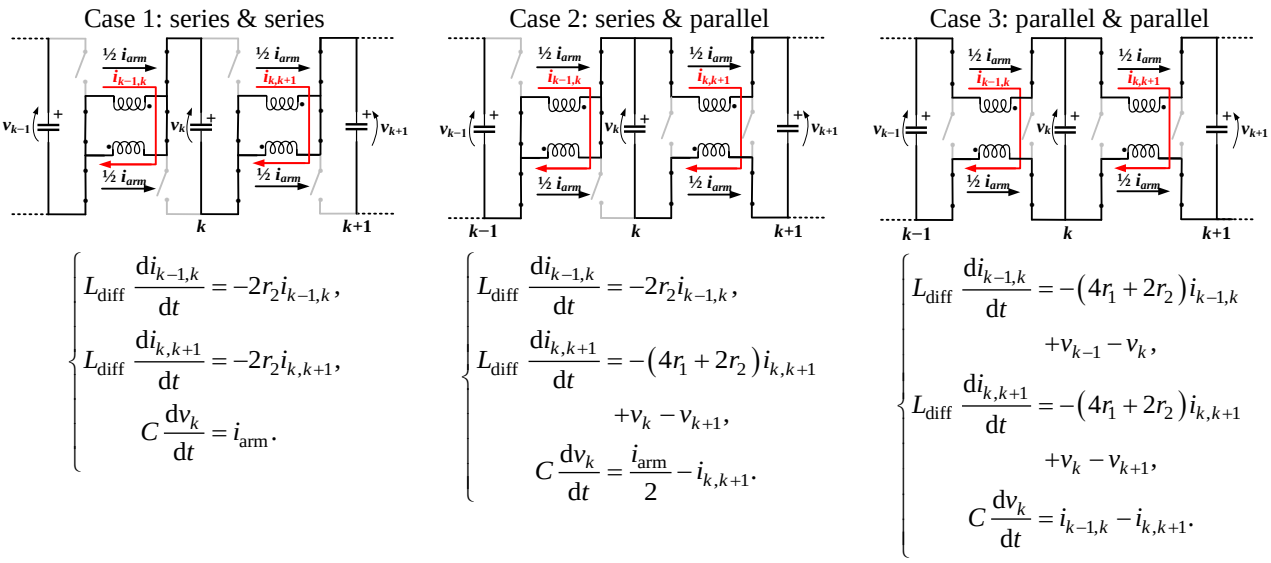


Fig. 2. Dynamics and current distribution in interconnections for different combination of RSPM switching states. We focus on the kth capacitor and the two balancing chokes beside.

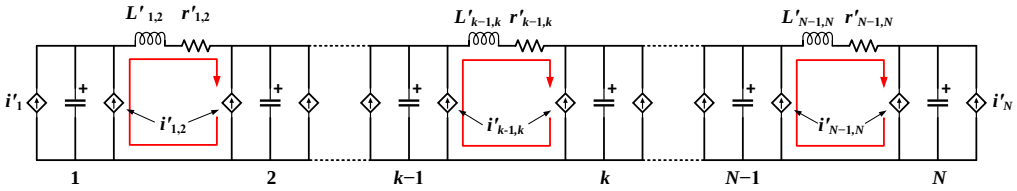


Fig. 3. Equivalent circuit of an RSPM string focusing on the balancing currents.

stability and the modulation method are presented in the next sections.

B. Balancing Currents

Upon parallelization, a large voltage difference between the capacitors can cause considerable surge current. To suppress the surge current, we add *balancing chokes* between the modules [Fig. 1(a)]. These balancing chokes are coupled inductors wired in such a way that they pass the arm current (i.e., common mode) but impede the balancing currents (i.e., differential mode). With a proper modulation scheme (Section II-C), the load is evenly split among modules and the voltage spread can only grow slowly. The balancing choke can have a small core. If the balancing choke is not coupled, its common-mode inductance can offset the arm inductors.

Alternatively, if a high switching frequency is allowed, the capacitor voltage difference never accumulates to a significant value. The balancing current can then be tolerable without balancing chokes. In this setting, the two middle switches can be merged, reducing the RSPM to a five-switch module [bottom part of Fig. 1(a)]. We analyze the balancing currents and losses below.

Without balancing chokes. During the switching period of $1/f_{\mathrm{sw}}$, the voltage difference accumulates up to $i_{\mathrm{arm}}/Cf_{\mathrm{sw}}$. A parallel state in the next switching cycle causes a peak balancing current of

$$i_{\mathrm{balance}} = i_{\mathrm{arm}} \big/ \left(rCf_{\mathrm{sw}}\right), \tag{2}$$

and balancing energy loss

$$E_{\mathrm{balance}} = \Sigma E_{\mathrm{cap,\,old}} - \Sigma E_{\mathrm{cap,\,new}} = {i_{\mathrm{arm}}}^2 \big/ \left(4Cf_{\mathrm{sw}}^2\right) \tag{3}$$

where i_{arm} refers to the arm current, C the module capacitance, and r lumps all resistance in the balancing path together. Equation (3) focuses on two modules during parallelization but the proportionality $E_{\mathrm{balance}} \propto {i_{\mathrm{arm}}}^2/(f_{\mathrm{sw}}{}^2C)$ is universal [18]. It is therefore effective to reduce the balancing loss by increasing the switching frequency f_{sw} or the module capacitance C. The dependence on the switching frequency is evidenced by experimental results in Fig. 13.

With balancing chokes. For medium-/high-voltage applications, the peak balancing current endangers the semiconductors because of the restricted switching frequency and the low resistance at the transistors and the capacitors. In these cases, balancing chokes are necessary. We follow a method in [19] to derive the internal system dynamics for this case. There are three basic combinations of the series− and parallel states (see Fig. 2 , series+ leads to the same conclusion due to symmetry). Defining $m_{k-1,k}$ as the duty cycle of the series state at the switching site L_k, the time-average dynamics is

$$\begin{cases} L'_{k,k+1}\dfrac{\mathrm{d}\bar{i}_{k,k+1}}{\mathrm{d}t} = -r'_{k,k+1}\bar{i}_{k,k+1} + v_k - v_{k+1}, 1 < k < N-1 \\ C\dfrac{\mathrm{d}v_k}{\mathrm{d}t} = i'_{k-1,k} + i'_{k,k+1} + \bar{i}_{k-1,k} - \bar{i}_{k,k+1}, \end{cases} \tag{4}$$

with

$$\begin{cases} L'_{k-1,k} \overset{\mathrm{def}}{=} \dfrac{L_{\mathrm{diff}}}{\left(1-\left|m_{k-1,k}\right|\right)^2},\ i'_{k-1,k} \overset{\mathrm{def}}{=} \frac{1}{2}\left|m_{k-1,k}\right| i_{\mathrm{arm}}, \\ r'_{k-1,k} \overset{\mathrm{def}}{=} \dfrac{4r_1+4r_2}{\left(1-\left|m_{k-1,k}\right|\right)^2},\ \bar{i}_{k-1,k} \overset{\mathrm{def}}{=} \left(1-\left|m_{k-1,k}\right|\right) i_{k-1,k}. \end{cases} \tag{5}$$

In Eqs. (4)–(5), the effects of the arm current are modeled as controlled current sources in parallel to the capacitors. In cascaded H-bridges, balancing can only be achieved by keeping $\int i'_1 + i'_{1,2}\,\mathrm{d}t = \int i'_{k-1,k} + i'_{k,k+1}\,\mathrm{d}t = \int i'_{N-1,N} + i'_N\,\mathrm{d}t$, which requires voltage monitoring and closed-loop control. In RSPMs, the differential current $i_{k-1,k}$ arises in parallel states and is driven by capacitor voltage differences. While the balancing choke keeps $i_{k-1,k}$ relatively constant, the actual charge-exchange rate is modulated by the average dwell time in the parallel state, thus $(1 - |m_{k-1,k}|)i_{k-1,k}$. Despite the autonomous balancing, it is recommended to roughly equalize the capacitor loads i_1', i_2',…, i_N' to minimize the balancing stress on the chokes; according to Eq. (5), this amounts to unifying $m_{k-1,k}$'s.

We derive the dynamics for the terminal modules to complete the circuit analysis. Note that the terminal switching site L_N only supports bypass+/− [Fig. 1(b)]. Similar to the above derivations, we define $|m_{N,1}|$ as the duty ratio in series states but split the rest of the duty ratio into $d\cdot(1 - |m_{N,1}|)$ for bypass+ and $(1 - d)\cdot(1 - |m_{N,1}|)$ for bypass−. As such,

$$\begin{cases} C\dfrac{\mathrm{d}v_1}{\mathrm{d}t} = i'_1 + i'_{1,2} - \bar{i}_{1,2}, \\ C\dfrac{\mathrm{d}v_N}{\mathrm{d}t} = i'_N + i'_{N-1,N} + \bar{i}_{N-1,N}, \\ i'_1 = \frac{1}{2}|m_{N,1}|i_{\mathrm{arm}} + \frac{1}{2}(2d-1)\left(1-|m_{N,1}|\right)i_{\mathrm{arm}}, \\ i'_N = \frac{1}{2}|m_{N,1}|i_{\mathrm{arm}} + \frac{1}{2}(1-2d)\left(1-|m_{N,1}|\right)i_{\mathrm{arm}}. \end{cases} \tag{6}$$

According to Eqs. (5)–(6) and the equivalent circuit, setting d = 0.5 and $m_{N,1} = m_{k-1,k} = m$ (k = 2, …, N) amounts to equalizing the capacitor load share, which minimizes the balancing currents. In this case, the output voltage is simply $v_{\mathrm{arm}} = mNV_{\mathrm{dc}}$.

C. Modulation

The above derivations suggest equal references for all switching sites for load-sharing purposes. As such, the modulation of RSPMs is almost identical to that of CHBs. Take phase-shifted carrier (PSC) scheme as an example [23], the main differences are *1)* the RSPM switching states are defined for interconnections instead of for modules, *2)* the parallel state is used at most interconnections instead of the bypass state. These differences only entail minor changes at the switching code book, which mostly involves static combinatorial logics. Similar to CHB, each RSPM switching site L_k (k = 1, 2, …, N) is paired with two unipolar carriers C_k^+ and C_k^- ($C_k^+ = -C_k^-$). The modulation rule is

$$s(L_k) = \begin{cases} m \ge C_k^+ : \text{series}+ \\ m \le C_k^- : \text{series}- \\ C_k^- < m < C_k^+ \text{ and } k = N : \text{bypass}\pm \\ C_k^- < m < C_k^+ \text{ and } k \ne N : \text{parallel}, \end{cases} \tag{7}$$

where m is the modulation reference shared by all switching sites of the same arm. The terminal switching site L_N takes bypass+ and bypass− alternatively when $C_k^- < m < C_k^+$ in order to effect d = 0.5. This toggling rule for L_N, together with the uniformed modulation index m, assures matched capacitor loads as per Eqs. (4), and (6). The PSC modulation for RSPM assigns parallel state in a cycling pattern through all switching sites to ensure charge-balancing across the entire arm. Even for large modulation indices, the modulator scans through RSPMs with at least one parallel state at the carrier frequency (Fig. 4).

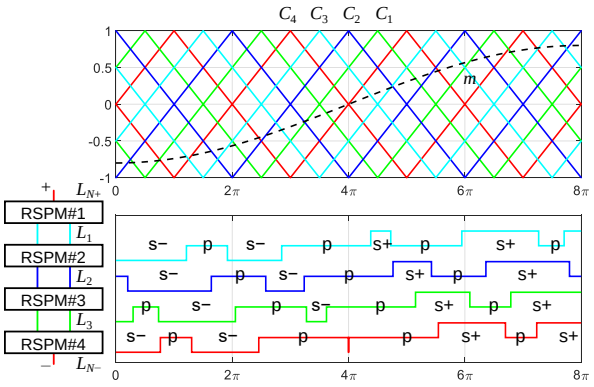


Fig. 4. PSC modulation scheme for a cascaded RSPM with four modules.

The above modulation scheme assures sensorless balancing and the same output quality as CHBs. One can, optionally, further improve the conduction loss by permutating the carrier sequence—an interesting control redundancy that can be exploited by series/parallel modules [19]. The key idea is that, instead of a trivial assignment C_1-L_1, C_2-L_2, C_3-L_3, C_4-L_4, C_5-L_5, C_6-L_6, a permutation such as C_1-L_1, C_3-L_2, C_5-L_3, C_2-L_4, C_4-L_5, C_6-L_6 (for N = 6) tends to parallelize RSPMs in evenly-sized groups under the proposed PSC scheme. Compared to a large parallel group with single RSPMs in series, a string of evenly paralleled groups generates better load-balancing and lower conduction loss. In this paper, we focus on N = 4 modules per arm. The corresponding optimal carrier assignment occurs to be C_1-L_1, C_2-L_2, C_3-L_3, C_4-L_4. For more modules in an arm, the optimal permutation is nontrivial (e.g., for N = 6 above), and we refer to [19] for more details.

III. Analysis

A. Balancing Dynamics

To evaluate the stability and the speed of the intrinsic balancing, we combine Equations (4)–(6),

$$\frac{d}{dt}\begin{bmatrix}\mathbf{v}\\ \mathbf{i}\end{bmatrix} = \underbrace{\begin{bmatrix}\mathbf{0} & \frac{1}{C}\mathbf{A}\\ \frac{1}{L'}\mathbf{B} & -\frac{r'}{L'}\mathbf{I}\end{bmatrix}}_{\mathbf{x}}\cdot\underbrace{\begin{bmatrix}\mathbf{v}\\ \mathbf{i}\end{bmatrix}}_{\mathbf{D}} + \frac{1}{C}\begin{bmatrix}\mathbf{i}'\\ \mathbf{0}\end{bmatrix}, \tag{8}$$

where vector $\mathbf{v}_{N\times 1}$ gathers the capacitor voltages, $\mathbf{i}_{(N-1)\times 1}$ gathers the inter-module circulating currents, and $\mathbf{i}'_{N\times 1}$ represents the shared load seen by each capacitor. The system dynamics are quantified by matrices **A**, **B** below, whereas **I** is the identity matrix of appropriate dimensions.

$$\underset{N\times(N-1)}{\mathbf{A}} = \begin{bmatrix} -1 & & & \\ 1 & -1 & & \\ & \ddots & \ddots & \\ & & 1 & -1 \\ & & & 1 \end{bmatrix}, \quad \underset{(N-1)\times N}{\mathbf{B}} = \begin{bmatrix} 1 & -1 & & \\ & \ddots & \ddots & \\ & & 1 & -1 \end{bmatrix}. \tag{9}$$

Eq. (8) tracks the capacitor voltages under the disturbance of $\mathbf{i}'$. While the proposed modulation method roughly equalizes the entries in $\mathbf{i}'$, any accumulative error will be cleared by the dynamics of Eq. (8) to ensure balance. We perform eigenvalue

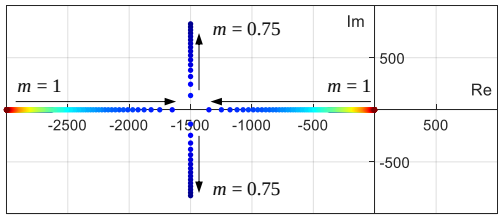


Fig. 5. Eigenvalues with $0.75 < m < 1$. We set $N = 3$ to be able to visually separate the eigenvalues. The other parameters are listed in TABLE I.

decomposition on matrix **D** and trace the evolution of system states **x** in absence of the disturbance **i**′.

For any $|m| < 1$, the only zero eigenvector is $\mathbf{x}_0 = [\mathbf{v}^{\mathrm{T}}, \mathbf{i}^{\mathrm{T}}]^{\mathrm{T}}$ with $v_1 = \ldots = v_N$ in **v** and **i** = **0**. This is easily understandable since such $\mathbf{x}_0$ represents balanced equilibrium, thus $d\mathbf{x}_0/dt = \mathbf{0} = \mathbf{D}\mathbf{x}_0$. The other eigenvalues are in the left half of the complex plane, as is shown in Fig. 5. Denoting λ as any non-zero eigenvalue for eigenvector $\mathbf{x}_\lambda$ yields

$$\frac{d\mathbf{x}_\lambda}{dt} = \lambda \mathbf{x}_\lambda \Rightarrow \mathbf{x}_\lambda(t) = e^{\mathrm{Re}(\lambda)t} e^{j\,\mathrm{Im}(\lambda)t} \mathbf{x}_\lambda(0). \tag{10}$$

Since $\mathrm{Re}(\lambda) < 0$, $\mathbf{x}_\lambda(t) \to 0$ as t increases; only $\mathbf{x}_0$ survives. In other words, any system state **x** will converge to its mean-value vector $\mathbf{x}_0$. Since the capacitor voltages **v** are included in **x**, the convergence to $\mathbf{x}_0$ proves the intrinsic balancing.

Also according to Eq. (10), the balancing speed is characterized by the largest time constant $\tau_{\max} = -1/\mathrm{Re}(\lambda_{\min})$, which depends on L' and m per Eq. (5). Notice that as $m(t) \to 1$, $L' \to \infty$, and hence $\tau_{\max} \to \infty$; such infinite balancing time is not a concern because for most of the time $m(t) < 1$. We further derive the upper bound of the capacitor voltage spread

$$\begin{aligned} &\max(\mathbf{v}) - \min(\mathbf{v}) \le \max(\mathbf{x}) - \min(\mathbf{x}) \le 2\|\mathbf{x}\|_\infty \\ &= 2\left\|\sum\nolimits_{\{\lambda\}} a_\lambda \mathbf{x}_\lambda\right\|_\infty \le 2\left\|a_{\lambda_{\min}} \mathbf{x}_{\lambda_{\min}}\right\|_\infty \\ &= e^{\mathrm{Re}(\lambda_{\min})t} \times 2\left\|a_{\lambda_{\min}} \mathbf{x}_{\lambda_{\min}}(0)\right\|_\infty \end{aligned} \tag{11}$$

where we first upper-bound the voltage spread $\max(\mathbf{v}) - \min(\mathbf{v})$ by L^∞-norm of the state vector **x**, which is then decomposed at its eigenvector-basis with coefficients a_λ. Component $\mathbf{x}_0$ is ignored throughout because it does not contribute voltage spread. The last inequality of (11) assumes sufficiently large t so that the slowest mode $\mathbf{x}_{\lambda\min}$ outlives the others. Considering the variability of m, we can derive the averaged time-constant for the balancing mechanism:

$$\tau = -\left(\frac{\omega}{2\pi}\int_0^{2\pi/\omega} \mathrm{Re}\,\lambda_{\min}(m(t))\,dt\right)^{-1} \tag{12}$$

The same analysis can be carried out for CHBs, whose system dynamics degenerate to $C d\mathbf{v}/dt = \mathbf{i}'$. Clearly, there are no intrinsic mechanisms to restore balance—the only leverage is modulation over the load share **i**′ [9]–[12], which require capacitor voltage information.

B. Influence on System Stability

In CHBs, the control bandwidth and stability are partly limited by the speed of the balancing methods [24], which is determined by measurement, sampling and communication speeds [25]. In contrast, the proposed topology balances

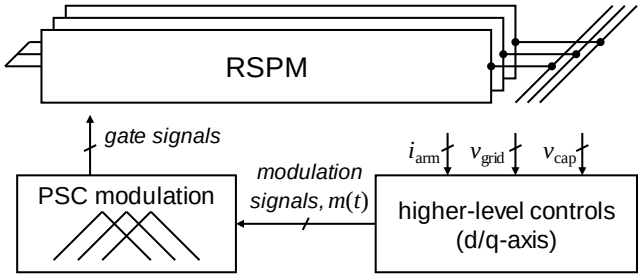


Fig. 6. Simplified control block diagram of the RSPM-STACOM. The scope of this paper is downstream from $m(t)$. Three capacitor voltage signals (one per arm) are required for cluster voltage control.

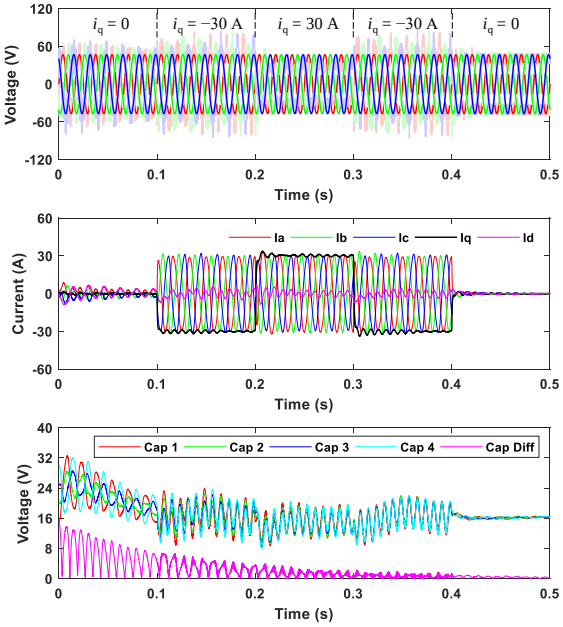


Fig. 7. Simulated capacitor voltages under extreme operating conditions. The parameters are listed in TABLE I. In the last panel, "Cap Diff" is calculated as $\max(\mathbf{v}) - \min(\mathbf{v})$.

modules at hardware level and does not interfere with any control loops. CHBs can be simply replaced by RSPMs without any adverse impact to the system stability. Thus, existing higher-level controls for CHBs can remain unchanged or possibly extended to even higher bandwidth. Fig. 6 shows the simplified control block diagram of the RSPM-STATCOM system. The proposed RSPM and modulation methods actualize the modulation signals. The higher-level controls may require average capacitor voltage for cluster voltage control. In light of the autonomous balancing, only one sensor per arm is required.

Finally, Fig. 7 shows the simulation results under several extreme operating conditions. These include a hard start-up with unequal module voltages followed by abrupt changes of the current reference. We do not optimize the higher-level control for these cases because they are irrelevant to the balancing performance. As predicted in Eq. (12), the capacitor voltage spread roughly follows the first-order decay despite the abrupt load changes.

C. Optimal Distribution of Transistor On-State Resistance

Compared to the original eight-switch SPM [18], the six-switch RSPM uses two transistors less per module while inheriting the same functionalities. The lower transistor count

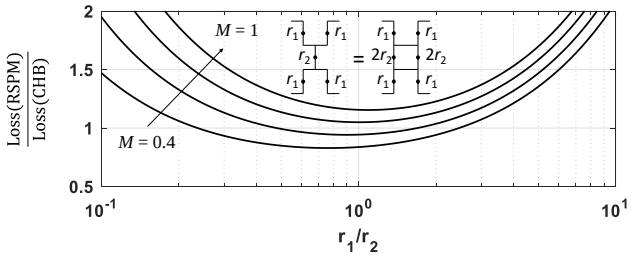


Fig. 8. Numerical results of the conduction loss ratio under various modulation depths M and transistor resistance ratios r_1/r_2. The definitions of on-state resistances r_1 and r_2 are shown.

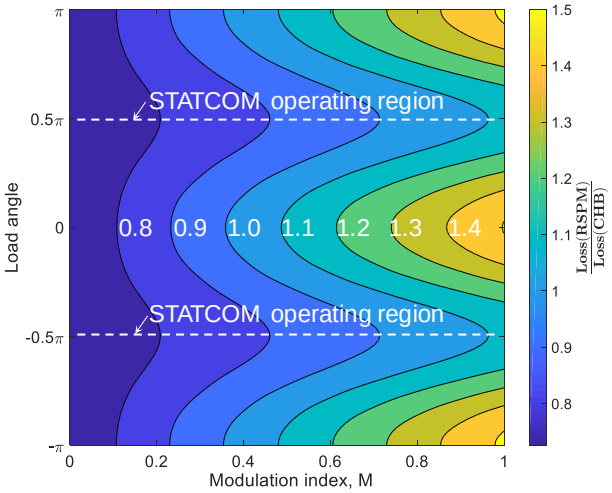


Fig. 9. Simulated conduction loss with various load angles and modulation indices M. The typical STATCOM operating region is marked.

reduces the circuit complexity. For STATCOMs where the power factor is zero, the series states only encounter low currents, whereas the parallel state distributes the current peaks across 2/3 transistors. As such, the additional switches of RSPM (compared to H-bridges) do not necessarily increase the conduction loss; rather, their silicon area can be traded for better conductivity at other switches, and thus an overall better efficiency. The optimal silicon budgeting is derived below.

At modulation index $m(t) = M\cos(\omega t)$ and arm current $i_{\text{arm}} = I\cos(\omega t + \pi/2)$, the conduction losses are

$$P_{\text{RSPM}} = \frac{1}{T}\int_0^T \underbrace{|m| i_{\text{arm}}^2 (2r_1 + r_2)}_{\text{series}\pm} + \underbrace{(1-|m|) i_{\text{arm}}^2 r_1}_{\text{parallel}}\, dt,$$
$$P_{\text{CHB}} = \frac{1}{T}\int_0^T \underbrace{|m| i_{\text{arm}}^2 (2r_{\text{CHB}})}_{\text{series}\pm} + \underbrace{(1-|m|) i_{\text{arm}}^2 (2r_{\text{CHB}})}_{\text{bypass}}\, dt. \quad (13)$$

If we further match the total semiconductor area for both cases

$$A = \frac{4}{r_1} + \frac{1}{r_2} = \frac{4}{r_{\text{CHB}}}, \quad (14)$$

the loss ratio $P_{\text{RSPM}}/P_{\text{CHB}}$ becomes a function of M and r_1/r_2. The numerical results in Fig. 8 show that the optimal ratio r_1/r_2 depends on M but is close to one. For simplicity, we suggest $r_1 = r_2$. With the same semiconductor budget, the RSPM achieves less conduction loss at $M < 0.7$ and at most 11.5% more loss at $M > 0.7$.

Fig. 9 compares RSPM and CHB under all combinations of the load angles and the modulation indices. The loss of the

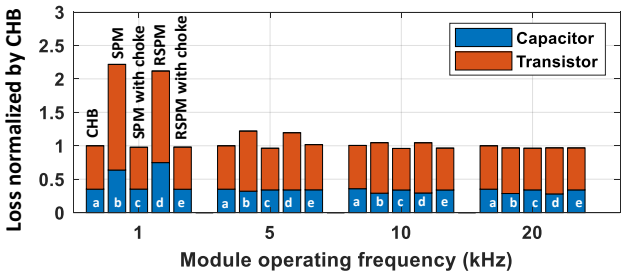


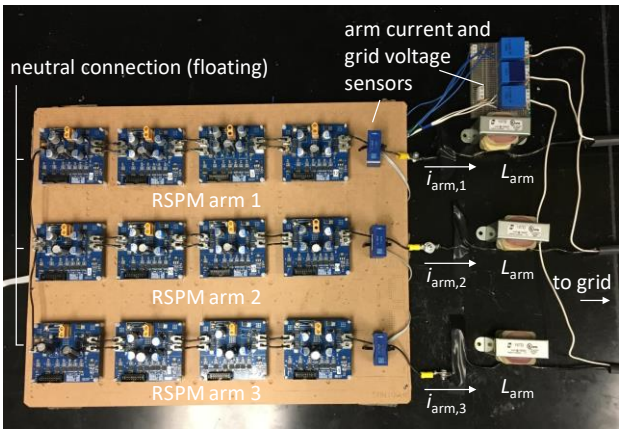
Fig. 10. Loss breakdowns for CHB, SPM, and RSPM. Four switching frequencies are compared. $M = 0.7$.

TABLE I
Setup settings

		Simulation	Experiment
Number of Modules	N	3 × 4	
Nominal module voltage	V_{dc}	40 V	17 V
Grid voltage (phase)*	V_{grid}	-	30 V
Grid frequency	f_{grid}	60 Hz	
Module capacitance	C	4 mF	
Transistor#1 on-state resistance	r_1	6.6 mΩ	
Transistor#2 on-state resistance	r_2		
Module switching frequency	f_{sw}	4 kHz	
Arm inductance	L_{arm}	1 mH	
Choke (if used)	L_{diff}	100 μH	16 μH @1 MHz

* obtained from a three-phase step-down transformer.

(a) RSPM setup, without balancing chokes



(b) wiring of the balancing chokes

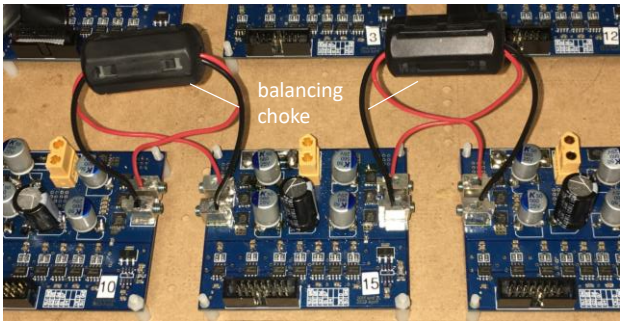


Fig. 11. Experimental setup of RSPM modules. (a) Overview. (b) Interconnection with balancing chokes.

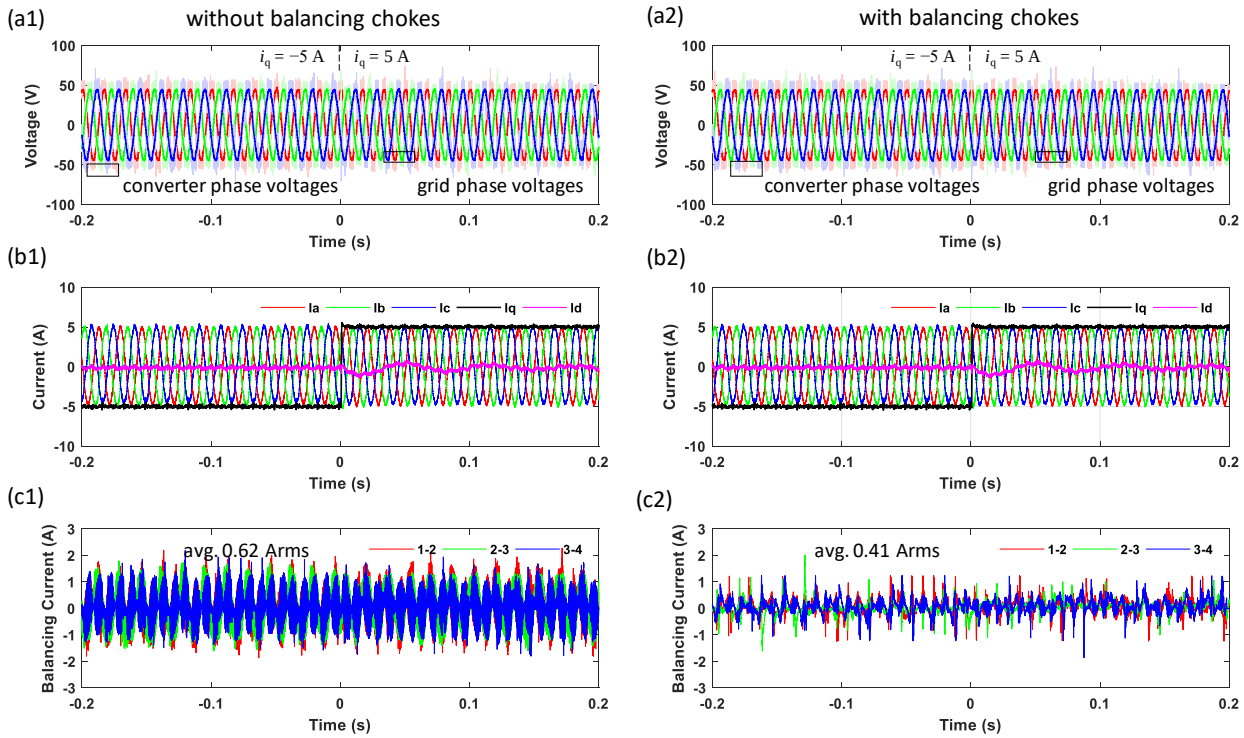


Fig. 12. Experimental results of the RSPM converter. (a) Converter output and grid voltages. (b) Output currents. (c) Balancing currents. Left column: without balancing chokes. Right column: with balancing chokes. At t = 0 s, i_q reference transits from −5 A to 5 A.

RSPM is minimized along the STATCOM's operating region (load angle = ± 0.5π) since the current apexes avoid passing through more silicon in series ($2r_1$ in series to r_2).

D. Loss Breakdown

The above results ignore the parallelization loss and assume even current sharing among the transistors. We further simulate detailed losses under different switching frequencies to provide more insights (Fig. 10). The total semiconductor area is matched across all evaluated topologies.

Without balancing chokes, both RSPM and SPM suffer large total conduction losses at low switching frequencies due to the surge balancing current. Increasing the switching frequency notably reduces the loss, rendering the RSPM and SPM even more efficient than the CHB. In part, the reduced loss owes to the load-sharing and thus lower capacitor loss [comparing (a) and (d) at 10–20 kHz in Fig. 10). Overall, the balancing chokes allow RSPM and SPM to efficiently operate at low switching frequencies, but the advantage is less prominent at higher switching frequencies.

IV. Experimental Results

A. Setup

We implement a three-phase down-scaled STATCOM to validate the proposed topology.[1] Each phase arm contains four RSPMs. Each RSPM is implemented with six MOSFETs that can operate without balancing chokes as in Fig. 11(a), or with balancing chokes as in Fig. 11(b). For the latter, we apply off-the-shelf EMI-suppression cores that present 16 μH differentially to the balancing current. The setup is controlled and modulated by an FPGA (sbRIO 9627, National Instruments). The parameters are detailed in TABLE I.

B. Control

We implement the classic decoupled d/q-axis control [26], [27], with the d-axis current controlling the cluster voltage and the q-axis current controlling the reactive power. Only one voltage sensor is implemented per arm for the cluster voltage control (near the middle of the arm; in this case, at the second module). As such, the inter-arm balancing is ensured by the information of the grid voltages and the modulation index; whereas the intra-arm module balancing is guaranteed by the series/parallel operation.

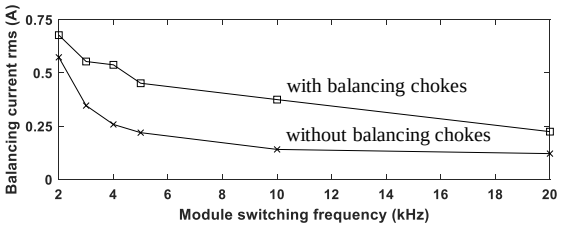


Fig. 13. Balancing current (in rms) with respect to the switching frequency.

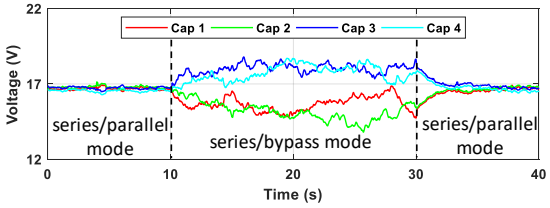


Fig. 14. Capacitor voltages over time. No balancing chokes are applied. The RSPM converter is switched to series/bypass mode for 20 seconds (to emulate typical CHBs) before returning to series/parallel mode.

[1] Please find data at https://osf.io/cjvpa/?view_only=a87a77888af8495fa634c909fe90684b

C. Results

Fig. 12 shows the waveforms during a transition from i_q = −5 A (providing 300 Var to the grid) to i_q = +5 A (consuming 300 Var) at t = 0 sec. Fig. 12(a1–c1) were obtained without balancing chokes, and Fig. 12(a2–c2) were obtained with balancing chokes at the same load condition. Comparing both sets of measurements, it is clear that the balancing chokes do not influence the arm-level dynamics but only suppress the balancing current. Without the balancing chokes, the average balancing current is 0.62 Arms, or 1.32% total conduction loss. Applying the balancing chokes halves the balancing current and reduces the parallelization loss to 0.58%. Fig. 13 further studies the influence of the switching frequency on the rms balancing currents. The balancing current drops roughly quadratically with respect to the switching frequency, validating Eq. (3).

Fig. 14 shows the capacitor voltages. During the first 10 seconds, the RSPM operates in the default mode with series and parallel states; during t = 10–30 sec, the modulator replaces the parallel state with bypass+/−, effectively emulating a CHB. As expected, the capacitor voltages diverge. At t = 30 sec, the modulator returns to the series/parallel mode to restore balance.

V. Conclusion

A reduced series/parallel module (RSPM) is proposed and optimized for cascaded multilevel STATCOMs. Compared to the conventional H-bridge modules, the additional switch in RSPM allows parallel interconnection, and cycling the parallel state throughout the arm guarantees sensorless balancing. The advantages of the proposed method are summarized below.

- It balances the modules at hardware level, which is completely autonomous. No voltage sensor is needed (except one per arm for the cluster voltage control), and the communication is greatly simplified.
- It guarantees balancing stability regardless of the load.
- It does not interfere with other control loops. Upgrading H-bridge modules to RSPMs is simple.
- It requires less components than similar series/parallel modules while achieving the same semiconductor utilization ratio as the H-bridge.

Reference

[1] P. Rao, M. L. Crow, and Z. Yang, "STATCOM control for power system voltage control applications," *IEEE Trans. Power Deliv.*, vol. 15, no. 4, pp. 1311–1317, 2000.

[2] M. Pereira, D. Retzmann, J. Lottes, M. Wiesinger, and G. Wong, "SVC PLUS: An MMC STATCOM for network and grid access applications," in *2011 IEEE PES Trondheim PowerTech: The Power of Technology for a Sustainable Society, POWERTECH 2011*, 2011, pp. 1–5.

[3] K. Frey, M. Garg, R. Morgenstern, N. Platt, and E. Spahic, "Provision of Fast Frequency Response by SVC PLUS Frequency Stabilizer," pp. 53 (6 pp.)-53 (6 pp.), 2019.

[4] T. Tanaka, K. Ma, H. Wang, and F. Blaabjerg, "Asymmetrical Reactive Power Capability of Modular Multilevel Cascade Converter Based STATCOMs for Offshore Wind Farm," *IEEE Trans. Power Electron.*, vol. 34, no. 6, pp. 5147–5164, 2019.

[5] P. H. Divshali and L. Soder, "Improving PV Dynamic Hosting Capacity Using Adaptive Controller for STATCOMs," *IEEE Trans. Energy Convers.*, vol. 34, no. 1, pp. 415–425, 2019.

[6] C. Han *et al.*, "STATCOM impact study on the integration of a large wind farm into a weak loop power system," *2006 IEEE PES Power Syst. Conf. Expo. PSCE 2006 - Proc.*, vol. 23, no. 1, pp. 1266–1272, 2006.

[7] C. Han, A. Q. Huang, Y. Liu, and B. Chen, "A generalized control strategy of per-phase DC voltage balancing for cascaded multilevel converter-based STATCOM," in *PESC Record - IEEE Annual Power Electronics Specialists Conference*, 2007, pp. 1746–1752.

[8] R. Xu *et al.*, "A novel control method for transformerless H-Bridge cascaded STATCOM with star configuration," *IEEE Trans. Power Electron.*, vol. 30, no. 3, pp. 1189–1202, 2015.

[9] Z. Liu, B. Liu, S. Duan, and Y. Kang, "A Novel DC Capacitor Voltage Balance Control Method for Cascade Multilevel STATCOM," *IEEE Trans. Power Electron.*, vol. 27, no. 1, pp. 14–27, 2012.

[10] J. Asakura and H. Akagi, "State-of-Charge (SOC)-Balancing Control of a Battery Energy Storage System Based on a Cascade PWM Converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1628–1636, Jun. 2009.

[11] M. Vasiladiotis and A. Rufer, "Analysis and Control of Modular Multilevel Converters with Integrated Battery Energy Storage," *IEEE Trans. Power Electron.*, vol. Early Acce, no. 1, pp. 1–1, 2014.

[12] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings*, 2003, vol. 3, pp. 272–277.

[13] A. Dekka, B. Wu, N. R. Zargari, and R. L. Fuentes, "A Space-Vector PWM-Based Voltage-Balancing Approach with Reduced Current Sensors for Modular Multilevel Converter," *IEEE Trans. Ind. Electron.*, 2016.

[14] A. Dekka, B. Wu, N. R. Zargari, and R. L. Fuentes, "Dynamic Voltage Balancing Algorithm for Modular Multilevel Converter: A Unique Solution," *IEEE Trans. Power Electron.*, 2016.

[15] K. Al-Haddad, R. Saha, A. Chandra, and B. Singh, "Static synchronous compensators (STATCOM): a review," *IET Power Electron.*, vol. 2, no. 4, pp. 297–324, Jul. 2009.

[16] Y. Jin, J. Wang, B. Xie, L. Li, and Y. Ji, "A diode-clamped cascaded H-bridge STATCOM for voltage balancing of individual capacitors," *Electr. Power Syst. Res.*, vol. 163, no. June, pp. 452–460, 2018.

[17] K. Ilves, F. Taffner, S. Norrga, A. Antonopoulos, L. Harnefors, and H. P. Nee, "A submodule implementation for parallel connection of capacitors in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3518–3527, Jul. 2015.

[18] S. M. Goetz, A. V. Peterchev, and T. Weyh, "Modular Multilevel Converter With Series and Parallel Module Connectivity: Topology and Control," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 203–215, Jan. 2015.

[19] Z. Li, R. Lizana, S. Sha, Z. Yu, A. V. Peterchev, and S. M. Goetz, "Module implementation and modulation strategy for sensorless balancing in modular multilevel converters," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8405–8416, 2019.

[20] Z. Li, R. Lizana, A. V Peterchev, S. Member, and S. M. Goetz, "Ripple Current Suppression Methods for Star- Configured Modular Multilevel Converters."

[21] S. M. Goetz, Z. Li, X. Liang, C. Zhang, S. M. Lukic, and A. V. Peterchev, "Control of Modular Multilevel Converter with Parallel Connectivity—Application to Battery Systems," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8381–8392, Nov. 2017.

[22] S. M. Goetz, Z. Li, A. V. Peterchev, X. Liang, C. Zhang, and S. M. Lukic, "Sensorless scheduling of the modular multilevel series-parallel converter: Enabling a flexible, efficient, modular battery," in *Conference Proceedings - IEEE Applied Power Electronics Conference and Exposition - APEC*, 2016, vol. 2016-May, pp. 2349–2354.

[23] Z. Li, R. Lizana, A. V. Peterchev, and S. M. Goetz, "Ripple current suppression methods for star-configured modular multilevel converters," in *Proceedings IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, 2017, vol. 2017-January, no. 1, pp. 1505–1510.

[24] S. Huang, R. Teodorescu, and L. Mathe, "Analysis of communication based distributed control of MMC for HVDC," in *2013 15th European Conference on Power Electronics and Applications, EPE 2013*, 2013, pp. 1–10.

[25] M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[26] M. S. El-Moursi and A. M. Sharaf, "Novel controllers for the 48-pulse VSC STATCOM and SSSC for voltage regulation and reactive power compensation," *IEEE Trans. Power Syst.*, 2005.

[27] H. M. El-Zoghby and A. F. Bendary, "Experimental Voltage Stabilization of a Variable Speed Wind Turbine Driving Synchronous Generator using STATCOM based on Genetic Algorithm," *Int. J. Emerg. Electr. Power Syst.*, 2016.

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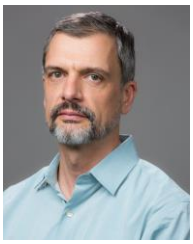

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