A Modular Multilevel Series/Parallel Converter for Wide Frequency Range Operation

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***Abstract*—When providing ac output, modular multilevel converters (MMCs) experience power fluctuation in the phase arms. The power fluctuation causes voltage ripple on the module capacitors, which grows with the output power and inversely to the output frequency. Thus, low-frequency operations of MMCs, e.g., for motor drives, require injecting common-mode voltages and circulating currents, and strict dc voltage output relative to ground is impossible. To address this problem, this paper introduces a novel module topology that allows parallel module connectivity in addition to the series and bypass states. The parallel state directly transfers power across the modules and arms to cancel the power fluctuations and hence suppresses the capacitor voltage ripple. The proposed series/parallel converter can operate at a wide frequency range down to dc without common-mode voltages or circulating currents; it also allows sensorless operation and full utilization of the components at higher output frequencies. We present detailed simulation and experiment results to characterize the advantages and limitations of the proposed solution.**

***Index Terms*—Modular-multilevel converter; voltage ripple; low-frequency operation**

I. Introduction

The modular multilevel converter (MMC) is one of the most promising voltage-source converters for medium- to high-voltage applications [1]–[8]. For medium-voltage motor drives [9]–[13], the low-voltage steps in the output of MMCs reduce the torque ripple [9], [14], the common-mode voltage [9], and the insulation stress on the motor windings [10], [15]. Despite these advantages, however, the MMC module capacitors experience low-frequency voltage ripple due to the oscillating power in the converter arms. The ripple amplitude increases with the load current [9], [12], [16] and is inversely proportional to the load frequency [9], [17]. This relation entails oversized module capacitors and challenges the use of MMCs in motor drives that require large torque at low and medium speeds [4], [18]–[20]. Indeed, MMCs are usually employed in applications where the output frequency is rather constant and the start-up current low. Examples include grid converters, mining machinery, cement mills, and pipeline pumps [9], [21]–[24].

A popular method to reduce the capacitor voltage ripple injects circulating currents across the MMC branches and common-mode voltage at the ac terminals. The product of both quantities transfers the low-frequency arm power to higher frequencies [4], [13], [25]–[29]. Various injection waveforms have been studied, including sinusoidal [29], [12], square [19], trapezoidal [30], and combinations thereof [27]. These methods are proven to be effective [9], [31] but suffer from the following drawbacks. First, the available common-mode voltage is restricted by the modulation index, and the effectiveness can be compromised by certain load conditions. Second, the common-mode voltage can produce leakage currents and stress the bearing, particularly for waveforms with high-frequency contents [32]. Third, the injected current produces additional loss, especially when the available common-mode voltage is small. Finally, the practicality of the injections is limited by the arm inductance, sensor sampling rates, and the control complexity [4], [19].

Alternative approaches for suppressing the capacitor voltage ripple implement physical power-transfer channels across the MMC arms, such as flying-capacitors [33] and auxiliary module strings [32]. Other studies add lateral power-transfer channels across different phases, including isolated module-to-module dc–dc converters [4], [34], [35] and delta-configured module strings [36]. With proper controls, these components cancel the module voltage ripple without imposing common-mode voltage at the loads. One potential downside is that the added power-transfer channels are under-utilized at rated output frequencies [32], indicating a potential lower round-trip efficiency or higher overall component cost. The additional components also demand dedicated control and sensors.

We propose a solution to achieve *1)* wide frequency range operations down to dc with less restriction on the modulation index, *2)* no common-mode voltage at the load, *3)* optional sensorless operation, and *4)* full component utilization at rated output frequencies. The key idea is to modify the MMC modules to allow parallel connection within and across the arms. The parallel connections serve as power-transfer channels to cancel the imbalanced arm powers. As a result, the capacitor voltages are kept near the nominal value regardless of the load size and frequency. With the series and parallel configurations, the proposed topology qualifies as a simplified modular multilevel series/parallel converter (MMSPC) [37] and is henceforth denoted as MMSPC in the remaining paper. Compared to the conventional MMC-based solutions [4], [13], [25]–[29], the MMSPC requires no common-mode voltage or arm-level circulating current and can operate at higher modulation indices. Compared to the solutions with cross-connection components [4], [32], [33], [36], [38]–[41], the MMSPC has a simpler physical structure, easier control implementation and maximum component utilization at rated output frequencies. However, the conduction loss of the power transfer through the parallel backbone increases if performed along a large number of modules, so that the proposed solution is used preferably in medium-voltage applications.

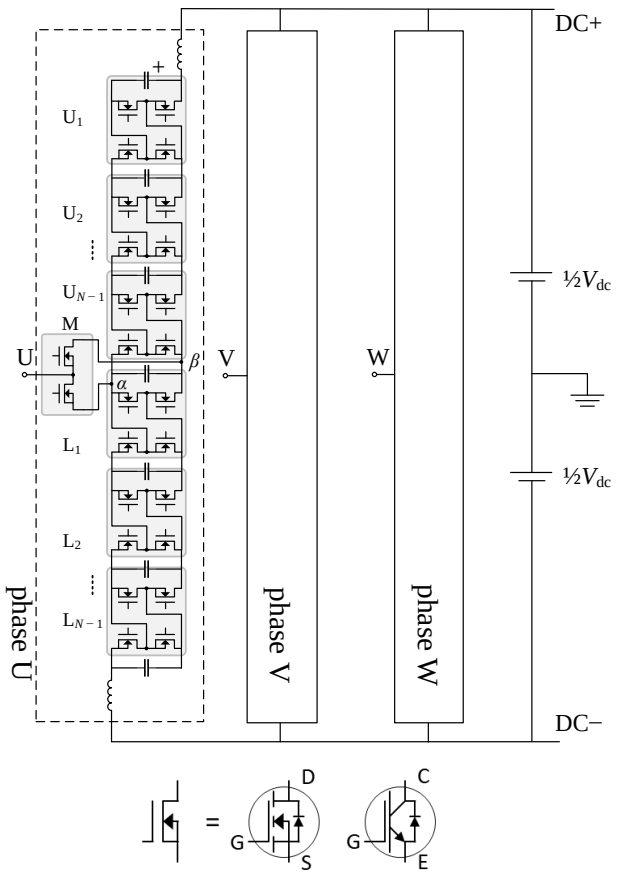

Fig. 1. The proposed modular multilevel series/parallel converter (MMSPC). Similar to the conventional MMCs, the number of the arm modules determines the quantization of the output voltage.

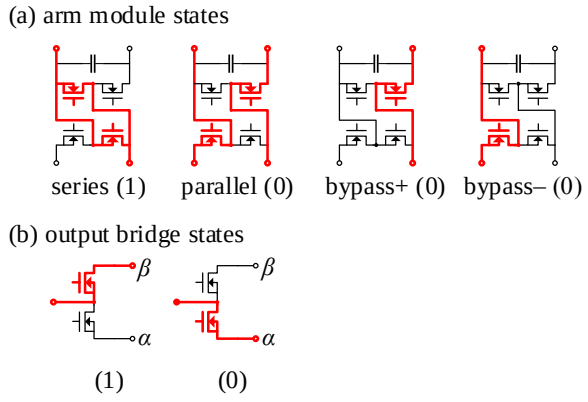

Fig. 2. Topology and basic switching states of (a) arm modules and (b) output bridges. The numbers in parentheses denote if a state increases the output voltage of the converter arm by a step (1) or not (0).

This paper is organized as follows. Section II introduces the module implementation and modulation principles. Section III analyzes the arm power and estimates the capacitor voltage ripples. Section IV studies the power losses of the proposed solution. Finally, Section V presents experimental results.

II. Modular Multilevel Series/Parallel Converter

A. Module Implementation and Switching States

Fig. 1 shows the MMSPC. With $2N - 1$ arm modules between the dc rails, the converter can produce voltage steps between $-N$ and $+N$. Each arm module consists of one capacitor, four transistors, and four terminals to connect to the adjacent modules. Each phase output is interfaced by a half-bridge module, henceforth called *output bridge*. The output bridges allow symmetric operation between the upper and lower converter arms. An output bridge increases the phase output voltage range in the same manner as adding two arm modules; as such, it has functions similar to the *middle cell* proposed for classical MMCs [17]. Alternatively, we can eliminate the output bridges and directly connect the ac output to either node α or β (Fig. 1). In this case, the modulation references for the respective arms should be offset. This topology reduction breaks the modulation symmetry but potentially saves the manufacturing effort. The module-balancing mechanisms remain the same in both configurations. Malfunctions in the output bridges can be compensated by the modulation references and will not disable the system. Without loss of generality, the following will implement the output bridge.

The MMSPC inherits the series and bypass states from the chopper (half-bridge) modules, but its additional terminals allow a parallel state [Fig. 2(a)]. The arm inductors are placed near the dc bus to make room for the parallel interconnections between the upper and the lower arms. The arm inductors are used to suppress the switching ripple and dc-fault currents and have similar dimensions as those of the conventional MMCs.

B. Modulation Framework and Operating Principle

The number of the arm modules in the series state determines the output voltage, whereas the locations of the bypass or parallel states influence balancing and load-sharing among the modules. Predictive controls give the best performances but are computationally expensive [37], [42]. Instead, this paper applies a previously proposed modulation method based on the phase-shifted carrier (PSC) framework [43], [44]. This modulation scheme uses the parallel state for power exchange, applies it instead of the bypass states wherever possible, and schedules it equally frequently for all switching sites. Specifically,

$$\begin{aligned}
\underset{k=1,\ldots,N-1}{state\ \mathrm{U}_k} &= \begin{cases} 1, & \text{if } ref_{\mathrm{U}} \geq 1-C_k, \\ 0, & \text{if } ref_{\mathrm{U}} < 1-C_k, \end{cases} \\
state\ \mathrm{M} &= \begin{cases} 1, & \text{if } ref_{\mathrm{M}} \geq C_N, \\ 0, & \text{if } ref_{\mathrm{M}} < C_N, \end{cases} \\
\underset{k=1,\ldots,N-1}{state\ \mathrm{L}_k} &= \begin{cases} 1, & \text{if } ref_{\mathrm{L}} \geq C_k, \\ 0, & \text{if } ref_{\mathrm{L}} < C_k, \end{cases}
\end{aligned} \tag{1}$$

where U_k is the kth upper-arm module; L_k is the kth lower-arm module; M is the output bridge; C_k is the phase-shifted carrier; and ref_{L}, ref_{U}, ref_{M} ($\in [0, 1]$) are the references. The numbers "1" and "0" indicate the switching states and follow the same convention of Fig. 2. The carriers of the upper arm are shifted by π with respect to those of the lower arm. Setting $ref_{\mathrm{L}} = ref_{\mathrm{M}} = 1 - ref_{\mathrm{U}}$ (derived later), the phase shift ensures a constant number of the activated modules (i.e., in series state) between

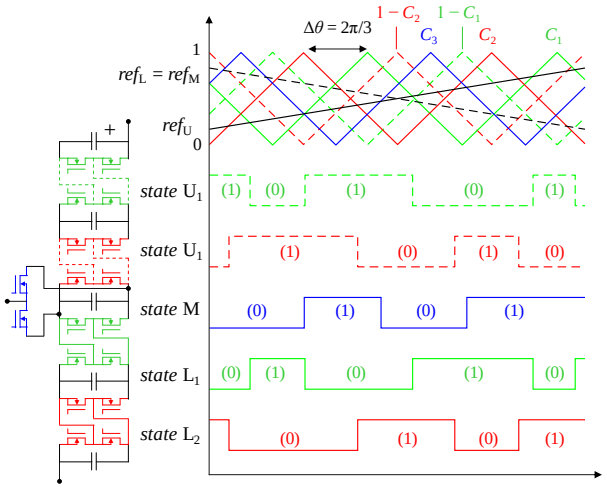

Fig. 3. An example of the modulation scheme for N = 3. The switching states are marked in the same convention as Fig. 2.

the dc rails and therefore minimal distortion on the dc side [45]. Despite involving more transistors than MMCs, the modulation method only selects between two switching states at each module by Boolean computations. Fig. 3 demonstrates the modulation scheme.

To derive the modulation references from the required ac output voltage, we assume constant and balanced capacitor voltages and neglect the voltage drop across the arm inductors. These assumptions are justified by the spontaneous module-balancing through the parallel interconnections and the absence of the additionally injected circulating currents. As such,

$$\begin{cases} v_x = V_{mdl} \times \left[(N-1) \times ref_L + ref_M \right] - \frac{1}{2} V_{dc}, \\ v_x = -V_{mdl} \times \left[(N-1) \times ref_U + 1 - ref_M \right] + \frac{1}{2} V_{dc}, \end{cases} \tag{2}$$

where V_{mdl} is the capacitor voltage. From Eq. (2)follows that

$$V_{mdl} = \frac{V_{dc}}{(N-1) \times (ref_U + ref_L) + 1}.$$

Eq. (3) indicates that the sum of the upper and lower arm references controls V_{mdl}. The denominator of the formula differs from that of the chopper-module MMCs by 1 because the top- and bottom-module capacitors are connected to the dc rails through different terminals. For example, in a hypothetical case of $ref_U = ref_L = 0$, all modules are paralleled, presenting one voltage step across the dc bus and therefore $V_{mdl} = V_{dc}$.

With Eqs. (2) and (3), one can calculate the required modulation references ref_U, ref_L, ref_M given the target capacitor voltage V_{mdl} and output voltage v_x. The remaining redundancy among ref_U, ref_L, ref_M will be used to partially reduce the low-frequency oscillating power in the converter arms.

III. Analysis

In both the conventional MMCs and MMSPCs, the upper and lower arms must provide second-order power and therefore create voltage ripple in the capacitors. However, in MMSPCs, the switched-capacitor-style parallel state between the modules and arms creates equalization currents to clear the voltage difference. Since the oscillating powers are of opposite phases between the upper and lower arms, an ideal exchange of the arm powers can contain the capacitor voltages in a narrow band, regardless of the output frequency. This section begins by analyzing the net power into each part of the converter to derive the optimal references ref_U, ref_L, and ref_M; it further derives a dc equivalent circuit to predict the required equalization currents.

A. Arm Power Fluctuation

For analysis purposes, we divide a phase branch into an upper section, a middle section, and a lower section. The middle section comprises the output bridge and any modules momentarily paralleled to it, and the upper and lower sections group the remaining modules (Fig. 6). At any switching state, the segmentation decouples the phase branch into three series-connected voltage sources: v_U (upper section), v_M (middle section), and v_L (lower section). The arm sections are related by

$$\begin{cases} i_U = i_Z + \frac{1}{2} i_x, \\ i_L = i_Z - \frac{1}{2} i_x, \\ v_U = V_{mdl} \cdot (N-1) \cdot ref_U, \\ v_L = V_{mdl} \cdot (N-1) \cdot ref_L, \\ v_M = V_{mdl}, \\ V_{dc} i_Z = v_x i_x, \end{cases} \tag{4}$$

where i_Z is the circulating current of the phase branch. The net input powers of the upper (p_U), lower (p_L) and middle (p_M) sections are

$$\begin{cases} p_U = v_U i_U = -p_\Delta - p_M \left(\frac{1}{2} + v_x / V_{dc} \right), \\ p_L = v_L i_L = +p_\Delta - p_M \left(\frac{1}{2} - v_x / V_{dc} \right), \\ p_M = V_{mdl} i_x \left(\frac{1}{2} + v_x / V_{dc} - ref_M \right), \end{cases} \tag{5}$$

$$p_\Delta = -i_x \left(V_{dc} - V_{mdl} \right) \left(\frac{1}{4} - v_x^2 / V_{dc}^2 \right). \tag{3}$$

The powers p_U, p_L, p_M sum to zero but independently drive the capacitor voltage ripples. We exploit the redundancy among ref_M, ref_U, ref_L and minimize

$$\min_{0 \le ref_M \le 1} \max \left\{ |p_U|, |p_L|, |p_M| \right\}, \tag{6}$$

under the constraints of Eqs. (2)–(3). The solution is (see Appendix A for details)

$$\begin{cases} ref_U = \frac{V_{dc} - V_{mdl}}{V_{mdl} (N-1)} \left(\frac{1}{2} - v_x / V_{dc} \right), \\ ref_M = \frac{1}{2} + v_x / V_{dc}, \\ ref_L = \frac{V_{dc} - V_{mdl}}{V_{mdl} (N-1)} \left(\frac{1}{2} + v_x / V_{dc} \right). \end{cases} \tag{7}$$

Further setting $V_{dc} = N V_{mdl}$, we obtain

$$ref_L = ref_M = 1 - ref_U = \frac{1}{2} + v_x / V_{dc}.$$

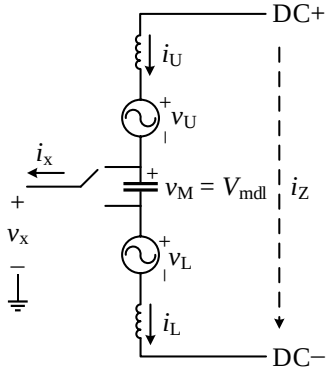

Fig. 6. Equivalent circuit of a single-phase MMSPC. The output bridge is modeled as an ideal switch interfacing the load.

Inserting Eq. (7) back into Eq. (5) yields

$$p_L = -p_U = p_\Delta, p_M = 0. \tag{9}$$

The optimization leverages the control redundancy on ref_M to reduce, but not completely cancel, the reactive power flow between the arms. The remaining oscillating arm power p_Δ should be mitigated by the parallel state through switched-capacitor-type power exchange, which is explained below. One can bypass the optimization of ref_M and define any modulation references per Eq.(2)–(3), and the parallel-state power-transfer channel can still eliminate the oscillating arm powers since $p_U + p_L + p_M = 0$; nevertheless, the internal loss will be higher due to the larger oscillating power and the consequently larger equalization currents between the modules.

B. Equivalent Circuit Model

This section derives an equivalent circuit to predict the capacitor voltages under dc output. We focus on the equalization current $i_{eq.}$ at the interconnection under the series and parallel switching states. We first consider a general case with stray inductance between the transistors [Fig. 4(a)], followed by a special case without the stray inductance [Fig. 4(b)]. These two cases do not differ in the circuit operation but influence the internal losses through different mechanisms. The internal losses are further explored in Section IV.

Case 1: with stray inductance. In the equalization-current loop [Fig. 4(b)], if the stray inductance is large enough so that the *R–L–C* resonance frequency is lower than the switching frequency, the circuit dynamics

$$\begin{cases} 2L_{stray}\dfrac{di_{eq.}}{dt} = -2r_{on}i_{eq.} & (\text{series}), \\ 2L_{stray}\dfrac{di_{eq.}}{dt} = v_{mdl,k} - v_{mdl,k+1} - 2r_{on}i_{eq.} & (\text{parallel}), \end{cases} \tag{10}$$

can be averaged into [46]

$$\begin{cases} v_{mdl,k} - v_{mdl,k+1} = L_{eq.U/L}\dfrac{di_{eq.}}{dt} + R_{eq.U/L}i_{eq.}, \\ L_{eq.U/L} = \dfrac{2L_{stray}}{1-ref_{U/L}}, \quad R_{eq.U/L} = \dfrac{2r_{on}}{1-ref_{U/L}}, \end{cases} \tag{11}$$

where r_{on} is the on-state resistance of the transistors, L_{stray} is the stray inductance, $i_{eq.}$ is the equalization current between the modules. Eq. (11) is further represented as an equivalent circuit

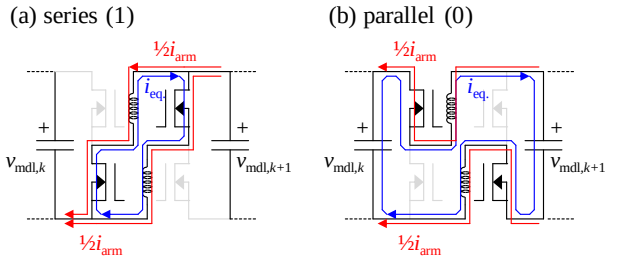

Fig. 4. Current distributions under series state (a) and parallel state (b). The stray inductance is shown.

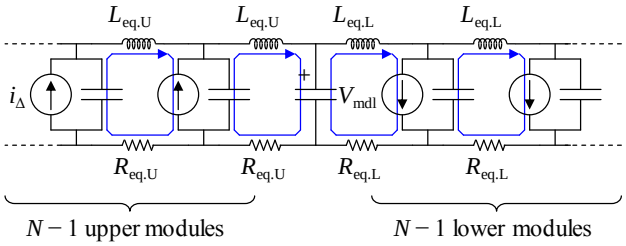

Fig. 5. Equivalent circuit model of the equalization current.

in Fig. 5. The circuit model shows how the capacitors are balanced under the oscillating power p_Δ, which is represented by virtual current sources $i_\Delta = p_\Delta/[(N-1)\ V_{mdl}]$ in parallel to the capacitors. The capacitor in the middle of the circuit is modeled as an ideal voltage source V_{mdl} because the output bridge is modulated such that $p_M = 0$ as in Eq. (9).

Case 2: without stray inductance. If the stray inductance is negligible so that $r_{on}/(2L_{stray}) >> f_{sw}$, the circuit is dominated by *R–C* dynamics. Suppose there is a voltage difference Δv between two adjacent modules, the parallel state transfers the following amount of charge:

$$\Delta Q = \frac{1}{2}\Delta v \cdot C\left[1-\exp\left(-\frac{1-ref_{U/L}}{Cf_{sw}r_{on}}\right)\right], \tag{12}$$

where C is the module capacitance. Similar to Case 1, we define

$$R_{eq,U/L} = \frac{\Delta v}{\Delta Q \cdot f_{sw}} \tag{13}$$

as a time-averaged measure of how the modulation scheme and transistors impede the equalization currents. As such, we can use the same dc circuit in Fig. 5 except $L_{eq,U/L} = 0$ to predict the capacitor voltages.

For both Case 1 and Case 2 under dc output, the steady-state capacitor voltages are given by

$$\begin{cases} v_{mdl,Uk} = V_{mdl} - \dfrac{k(2N-k-1)\,p_\Delta R_{eq,U}}{2(N-1)V_{mdl}}, \\ v_{mdl,Lk} = V_{mdl} + \dfrac{k(2N-k-1)\,p_\Delta R_{eq,L}}{2(N-1)V_{mdl}}, \end{cases} \tag{14}$$

where $v_{mdl,Uk}$ and $v_{mdl,Lk}$ are the k-th ($k = 1, \ldots, N-1$) capacitor voltages of the upper and lower arms, respectively.

The above analysis only considers the equalization current between the adjacent modules. In practice, the equalization current can go through multiple modules in parallel [47] and

further reduce the voltage imbalance in Eq. (14). However, we do not model the complete equalization currents for simplicity, and the circuit model overestimates the capacitor voltage distribution.

IV. Loss and Design Considerations

A. Simulation Models

We implement a single-phase MMC model and a single-phase MMSPC model in Matlab/Simulink to assess properties that are not available in the hardware setup. For comparability purposes, both models use the same number of modules and the same total semiconductor area, i.e., each MMSPC transistor has twice the on-state resistance as that of the MMC transistor (Table 1). All tests are performed with dc output unless otherwise noticed. The MMSPC model is operated with the proposed modulation method. The MMC model is controlled by the known method of injecting high-frequency sinusoidal current and common-mode voltage [26]–[29]. We maximize the MMC's common-mode voltage in order to minimize the required circulating current and thus the conduction loss.

B. Design Considerations

Fig. 7 studies how the module capacitance C, the stray inductance L_{stray}, the switching frequency f_{sw}, and the number of modules N influence the power-equalization loss. If the stray inductance is not negligible, increasing the design parameter Cf_{sw}^2 reduces the equalization loss and hence the overall conduction loss. The equalization loss inversely relates to Cf_{sw}^2 because Cf_{sw}^2 characterizes the ratio between the switching frequency and the R–L–C resonance frequency—fewer oscillations during the parallel state produce less loss on the transistors. If the stray inductance is negligible, the equalization loss is also inversely related to Cf_{sw}^2 because in this case the energy loss ΔE upon parallelization is given by [37]

$$\Delta E \propto C\Delta v^2 \propto \left(Cf_{\text{sw}}^2\right)^{-1}, \tag{15}$$

where Δv denotes the voltage difference between the adjacent capacitors before parallelization. Thus, this loss term also establishes an upper bound of the parallelization loss.

Overall, Fig. 7 indicates that the stray inductances as small as 50 nH can effectively reduce the conduction loss, even with small capacitance and low switching frequencies (e.g., $C = 1.5$ mF and $f_{\text{sw}} = 10$ kHz, see Fig. 7). Furthermore, the design choices of the capacitance, switching frequency, and stray inductance are not sensitive to the number of modules per arm, as the cases with $N = 4$ and $N = 8$ show similar loss-reduction trends.

Circuits in practice usually provide sufficient stray inductance. In fact, a 10-cm interconnection cable constitutes around 100 nH [48]. The commutation-loop inductance of a practical half-bridge circuit is usually above 100 nH, and insulated-gate bipolar transistor (IGBT) modules typically have package inductance of 15–75 nH [49]–[52]. Importantly, the stray inductance is not part of the switching-commutation loop and its current can always find freewheeling paths regardless of the momentary switching state or transitions across them. Dedicated inductors, such as distributed arm inductors, can be used to further smoothen the equalization currents without compromising the switching loss.

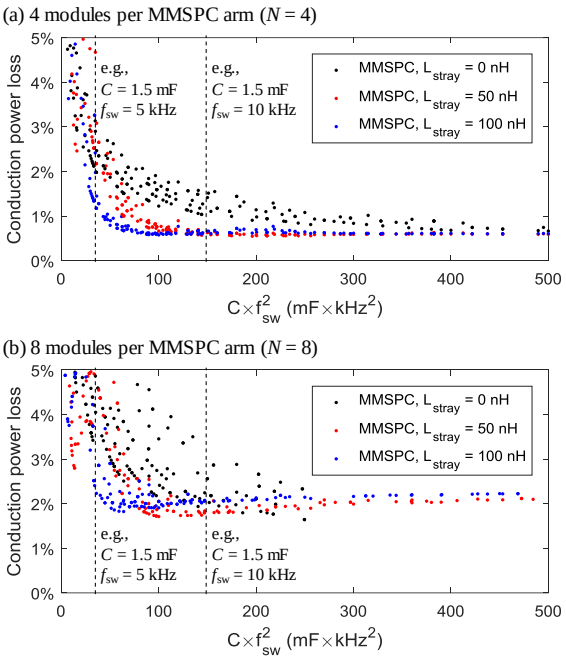

Fig. 7. Conduction loss of the MMSPC model with (a) 4 modules per arm and (b) 8 modules per arm. Each dot represents a random combination of L_{stray}, C, and f_{sw}. Table 1 lists the other parameters.

C. Converter Loss

Although some combinations of C, f_{sw}, and L_{stray} can suppress the peak equalization current, a minimum amount of the equalization current must exist to transfer the oscillating power. This section compares the efficiency of the proposed open-loop MMSPC versus a closed-loop MMC in simulations.

In Fig. 8(a), the MMSPC model with the proposed control presents higher conduction loss than the MMC at low modulation indices because the MMSPC's imbalanced arm powers are transferred through the parallel connections, which has the fixed port voltage V_{mdl} and consequently requires large equalization currents. On the other hand, the MMC's common-mode voltage can be multiples of V_{mdl} at low modulation indices and hence requires less circulating current to exchange the same power [19], [28]. At higher modulation indices (e.g., $m > 0.8$), the MMSPC model's loss does not increase much due to the fixed port voltage; whereas the MMC model's loss increases rapidly because of the smaller common-mode voltage and thus the higher circulating current.

Fig. 8(b) compares the loss of the two models with various numbers of modules per arm. The MMSPC model with the proposed control presents higher conduction loss than the MMC model at large N because the MMC's available common-mode voltage scales with the number of modules while the MMSPC's port voltage remains constant.

Fig. 8(c) compares the conduction loss under various load frequencies. For ac loads, we disabled the circulating current in the MMC model and kept the MMSPC model's control unchanged. When the load frequency is sufficiently high, the MMSPC module capacitors buffer a majority of the oscillating arm power, while the equalization currents diminish. Since the MMSPC has the same semiconductor amount as that of the MMC and that the MMSPC switches evenly share the arm

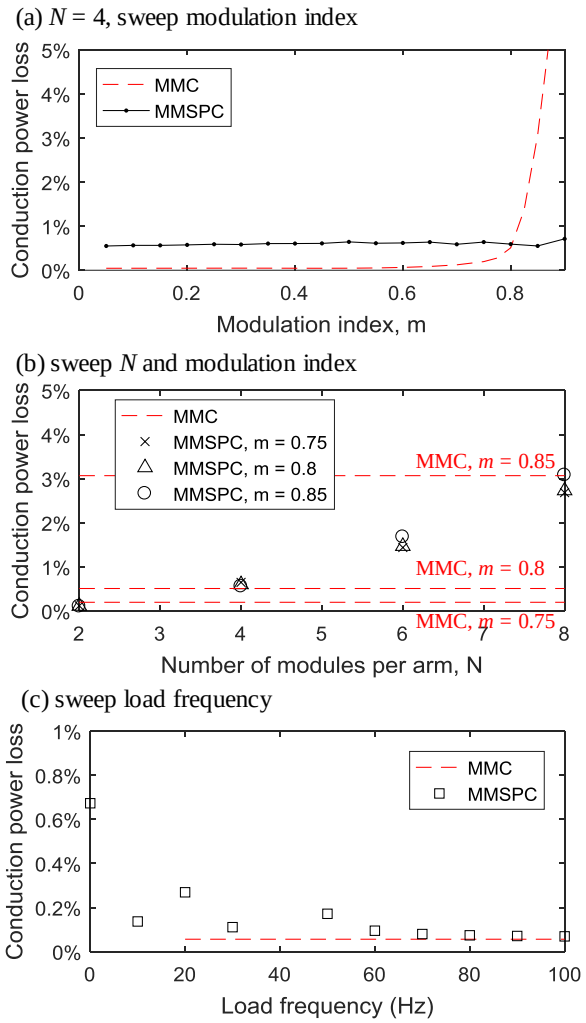

Fig. 8. Loss comparisons under (a) various modulation indices with the same load resistance, (b) various number of modules with the same load current, and (c) various load frequencies with other settings the same as Table 1. In subplot (c), the circulating current and common-mode voltage are disabled in the MMC, whereas the inter-arm power transfer is always activated in the MMSPC.

current (Fig. 4), both models produce the same loss at high output frequencies [37], [47]. Of course, the parallel switching state of the MMSPC can be disabled beyond certain load frequency to reach a higher round-trip frequency.

D. Application Range

The proposed MMSPC is suitable for medium-voltage motor drives where the dc bus voltage is lower than 10 kV and the number of modules per arm is less than ten [4], [12], [19], [31], [33], [53], [54]. For such low number of modules, MMSPCs with the proposed control can achieve higher dc efficiency than the conventional MMC-based solutions [26]–[29], particularly at high modulation depths. The presented solution is also preferable if the common-mode voltage is detrimental to the load. Furthermore, when ac output frequencies are considered, the proposed solution can have a higher round-trip efficiency or better component utilization than the methods using additional cross-arm power-transfer components [4], [32]–[36].

Table 1
Circuit parameters for experiments and simulations

	MMSPC	**MMC**
Nominal power	200 VA	200 VA
Output frequency	≥ 0 Hz	≥ 50 Hz *
No. of modules	7 arm modules + 1 output bridge	8 chopper modules
Module voltage	15.5 V	15.5 V
Module capacitance	1.5 mF	1.5 mF
No. of independent switches per module	4	2
Switch on-state resistance	0.4 mΩ	0.2 mΩ
Module switching frequency	5 kHz	5 kHz

* to keep the module voltage ripple below 0.15 p.u. (per unit value).

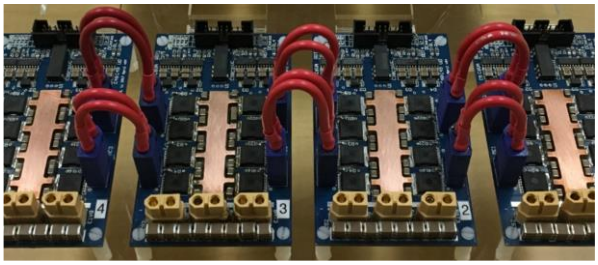

Fig. 9. Experimental setup of the MMSPC.

Finally, the MMSPC is simpler to control because *1)* the parallel power-transfer channel obviates closed-loop controls in inter- and intra-arm balancing, and *2)* the modulation scheme only chooses between two switching states (i.e., the series and parallel) by Boolean operations.

V. Experimental Results

A. Power Stage

The proposed solution was implemented and tested on a down-scaled single-phase setup (Fig. 9). The setup consists of seven modules and one output bridge. The transistors are implemented with silicon FETs. The module dc capacitor has C = 1.5 mF, or the unit capacitance constant of $\tau_c = NCV_{mdl}^2/S = 7.2$ kJ/MVA [55].

For comparison, an equivalent single-phase MMC with chopper modules was assembled with the same components but different inter-module wirings as the MMSPC setup. Each independent switch of the chopper module is implemented by two of the MMSPC transistors in parallel. The key parameters of the two systems are listed in Table 1.

B. Control Implementation

We use an FPGA (sbRIO 9627, 40 MHz clock rate, National Instruments) as the control platform. The MMC system is controlled by a standard method from the literature [43]. No common-mode voltage or circulating current was injected in either system, and no sensor was implemented in the MMSPC setup. Despite the sensorless control, there is no need to match the module capacitors because the equalization currents automatically occur to restore module balance.

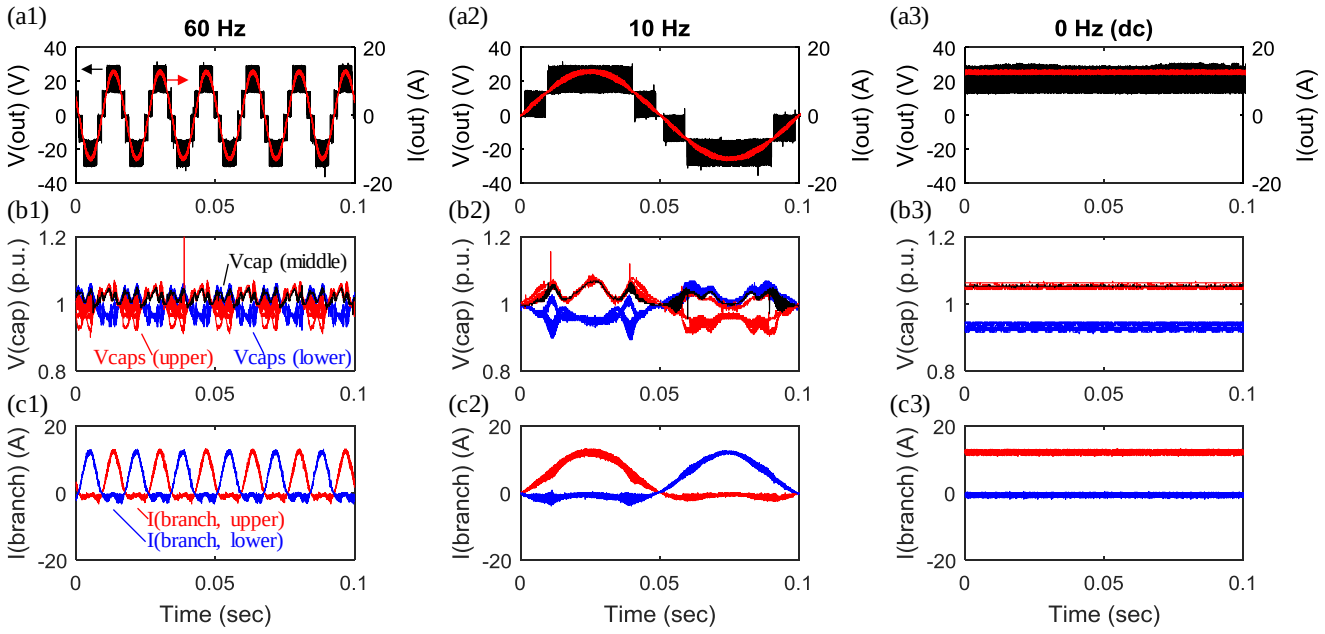

Fig. 10. Experimental waveforms of the MMSPC. (a1–3) Load voltage and load current. (b1–3) Capacitor voltages, where 1 p.u. corresponds to V_{mdl} = 15.5 V. (c1–3) Branch currents. Across the three cases the peak modulation index is 90% and the peak load current is set such that the unit capacitor constant is τ_c = 7.2 kJ/MVA.

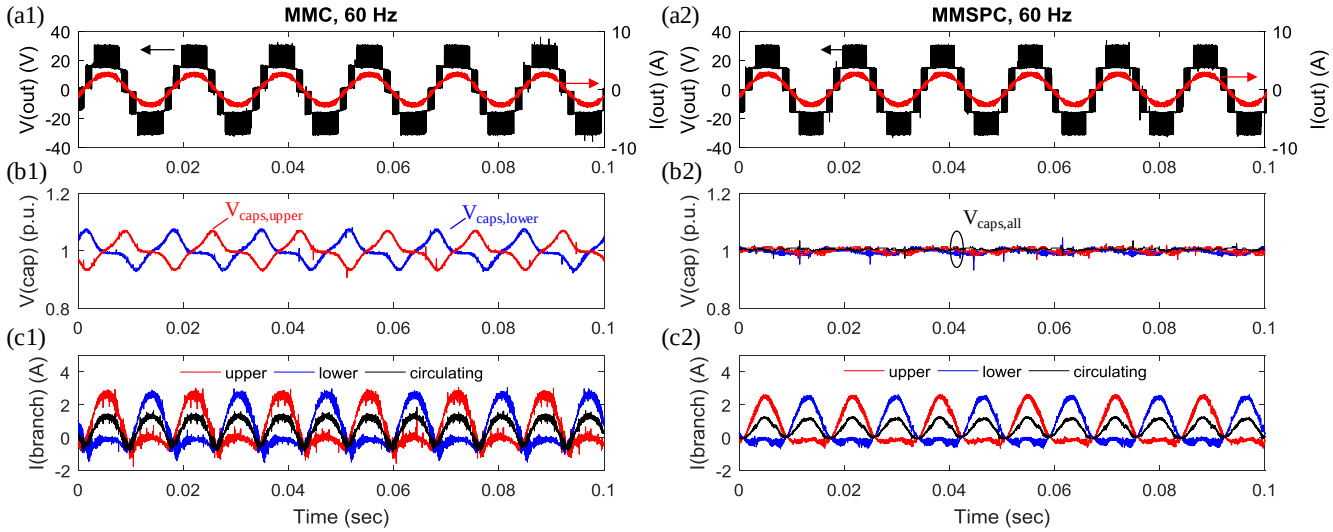

Fig. 11. Comparison between the MMC and the MMSPC. The load condition is the same. For the capacitor voltages, 1 p.u. corresponds to V_{mdl} = 15.5 V.

C. *Results*

Fig. 10 shows the capacitor voltage ripple of the MMSPC setup under various load frequencies. As predicted by Eq. (14), the peak capacitor voltage ripple is nearly independent of the load frequency. Despite the low capacitance (7.2 kJ/MVA), the system can operate at 0 Hz with the full load, while keeping the capacitor voltage ripple amplitude below 10%. The capacitor next to the output bridge presents smaller voltage ripple [Fig. 10(b), black lines] since this capacitor does not experience the low-frequency arm power according to Eq. (9).

To compare the MMC and MMSPC setups, the load was lowered to 25% of the nominal value to avoid damaging the MMC modules. At 60 Hz, Fig. 11 indicates that a typical MMC would require several times larger capacitance than the MMSPC for reaching the same ripple amplitude. Indeed, typical grid-connected MMCs have module capacitance of 40 to 110 kJ/MVA [16], [56]. Despite the different internal circuit dynamics, the MMSPC presents a similar branch current [Fig. 11(c2)] as that of the typical MMCs [57]. The branch current of the MMC setup [Fig. 11(c1)] is notably distorted because of the larger capacitor voltage ripple and has 11% larger rms value than that of the MMSPC setup even without circulating-current injections [1.28 A in Fig. 11(c1) versus 1.15 A in Fig. 11(c2)].

Fig. 12(a) summarizes the results of a frequency sweep between 0 Hz and 60 Hz. The line represents the prediction from Eq. (14). The MMSPC can suppress the voltage ripple with small capacitors in a manner largely independent of the output

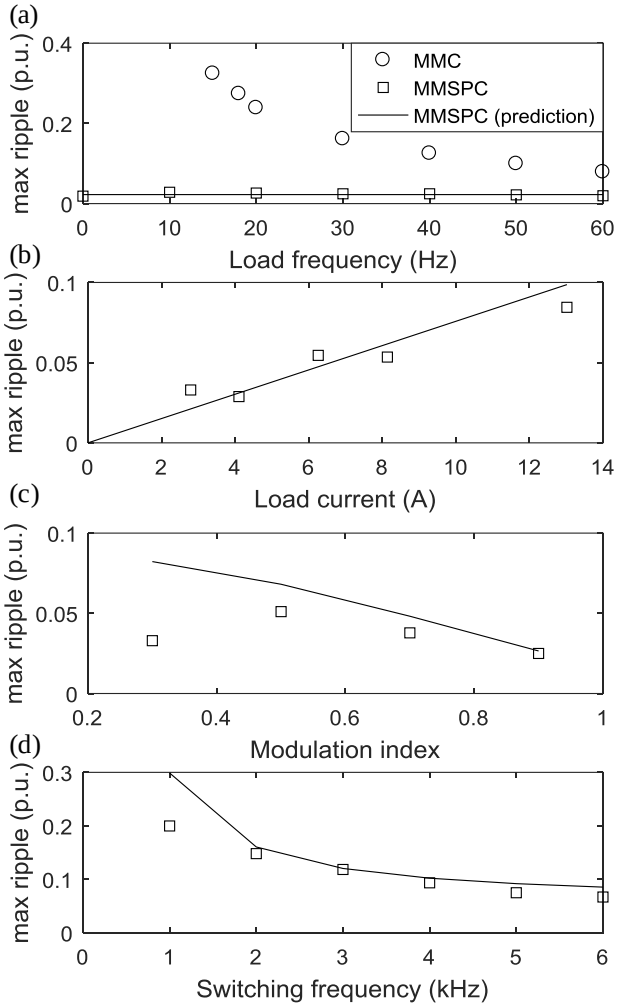

Fig. 12. Parameter study of the MMSPC module voltage ripple. (a) Influence of the load frequency. (b) Influence of the load current. (c) Influence of the modulation index with the load current fixed. (d) Influence of module switching frequency.

frequency. The ripple magnitude of the MMC setup, on the other hand, exhibits the known inverse proportionality to the load frequencies.

D. Parameter Study

We identified the following factors that influence the capacitor voltage ripple of the proposed converter.

1) Load conditions. Fig. 12(b) demonstrates a linear relationship between the ripple amplitude and the load power, in agreement with Eq. (14). Fig. 12(c) shows a nonmonotonic influence of the modulation index. The reason is that at higher modulation indices, the oscillating power p_Δ is mainly limited by the term $(¼ - v_x^2/V_{dc}^2)$ per Eq. (5), whereas at lower modulation indices, the load current i_x is smaller and keeps p_Δ small. Moreover, for lower modulation indices, the measurements show smaller capacitor voltage distribution than the predicted. The discrepancy occurs because the parallel connections can cover multiple modules and exchange more charge than Eqs. (10) and (12) would predict.

2) Module switching frequency and module capacitance. Fig. 12(d) shows the ripple amplitude versus the switching frequency. The two quantities are inversely related because at lower switching rates more unbalanced power is temporarily stored in the capacitors before released to the opposite arm. The stored energy then causes the capacitor voltage ripple. The discrepancy at $f_{sw} < 2$ kHz reflects our worst-case assumption that only two modules are involved in the power transfer each time. At higher switching rates, the discrepancy disappears because the capacitors are charged/discharged at a nearly constant rate, and how many modules are momentarily paralleled becomes less important. The cross-validation is shown in Fig. 13, where the measurements, simulation results, and theoretical predictions are enumerated by $\tau_C f_{sw}$ ($\propto C f_{sw}$), corresponding to the circuit analysis in Eq. (12).

E. Equalization and Capacitor Currents

Fig. 14 shows all equalization currents in the circuit. The dc modulation index is 0.5. The equalization currents reflect the switching behavior of the power transfer. Increasing the switching frequency or the module capacitance reduces the peak-to-peak current.

Fig. 15 shows the capacitor current waveforms with various switching frequencies and module capacitances. Similar to the equalization currents, increasing the switching frequency or the module capacitance helps reduce the peak capacitor current because larger capacitance decreases the resonant frequency of the power-transfer channel and thus stabilizes the equalization current. If we model the physical power-transfer channel as a single-turn rectangular coil with length = 12 cm, width = 3.5 cm, and wire diameter = 2 mm (12 AWG, see Fig. 9), the loop inductance is approximately 160 nH [48]. With 1.5-mF module capacitance, the loop inductance results in a resonant frequency of 10.2 kHz, matching the waveforms in Fig. 14 and Fig. 15. With 16.5-mF module capacitance, the resonant frequency becomes 3.1 kHz, allowing the module switching frequency to be lowered to 1–5 kHz without conducting the apex of the resonant currents.

The currents in Fig. 14 and Fig. 15 are measured by Fluke 80i-110s AC/DC current probes, which have the bandwidth of 0–100 kHz. The waveforms are recorded by a Tektronix MDO3054 oscilloscope at 400-ns resolution. The measurement instruments cover the highest-frequency contents during the parallelization (i.e., 10.2 kHz when the module capacitance is 1.5 mF) but may miss details of the reverse-recovery events during hard-switching. Limited by the number of the recording channels and current probes, some current waveforms are not

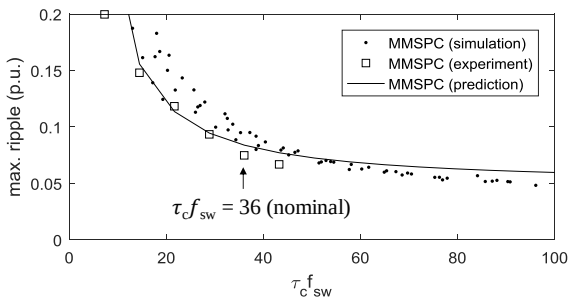

Fig. 13. The influence of the capacitance (represented by the unit time constant) and the switching frequency on the module voltage ripple. For each $\tau_c f_{sw}$, multiple combinations of τ_c and f_{sw} are simulated.

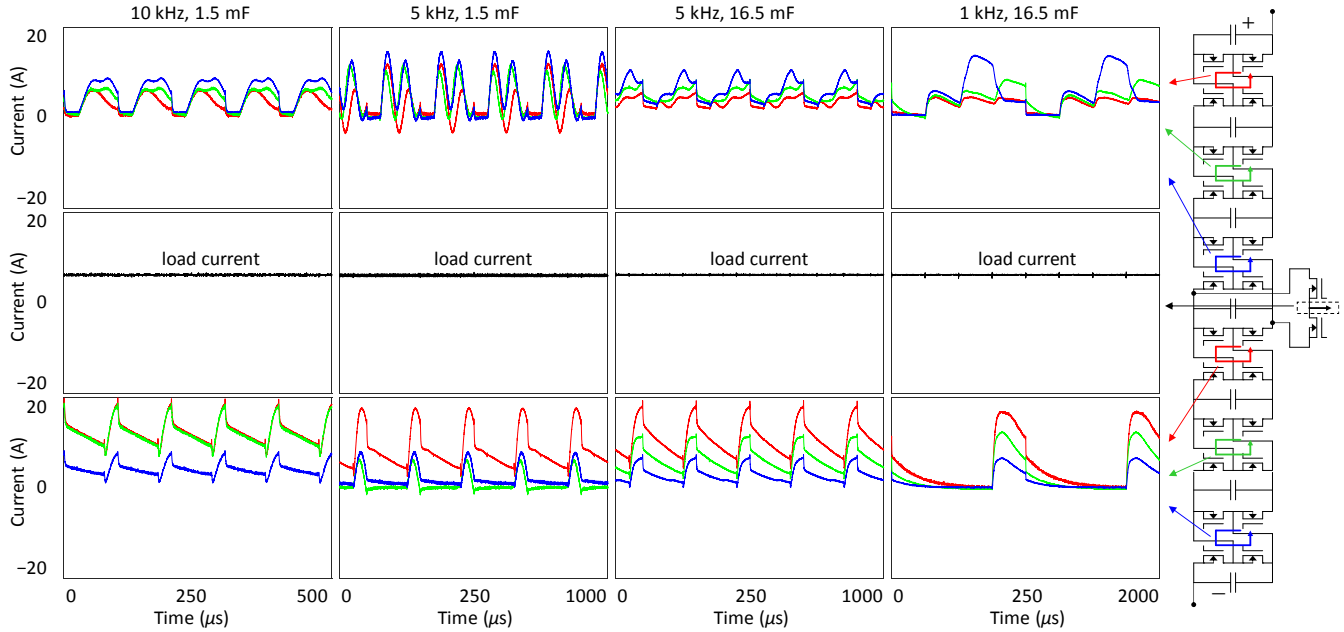

Fig. 14. Equalization currents for various switching frequencies and module capacitances.

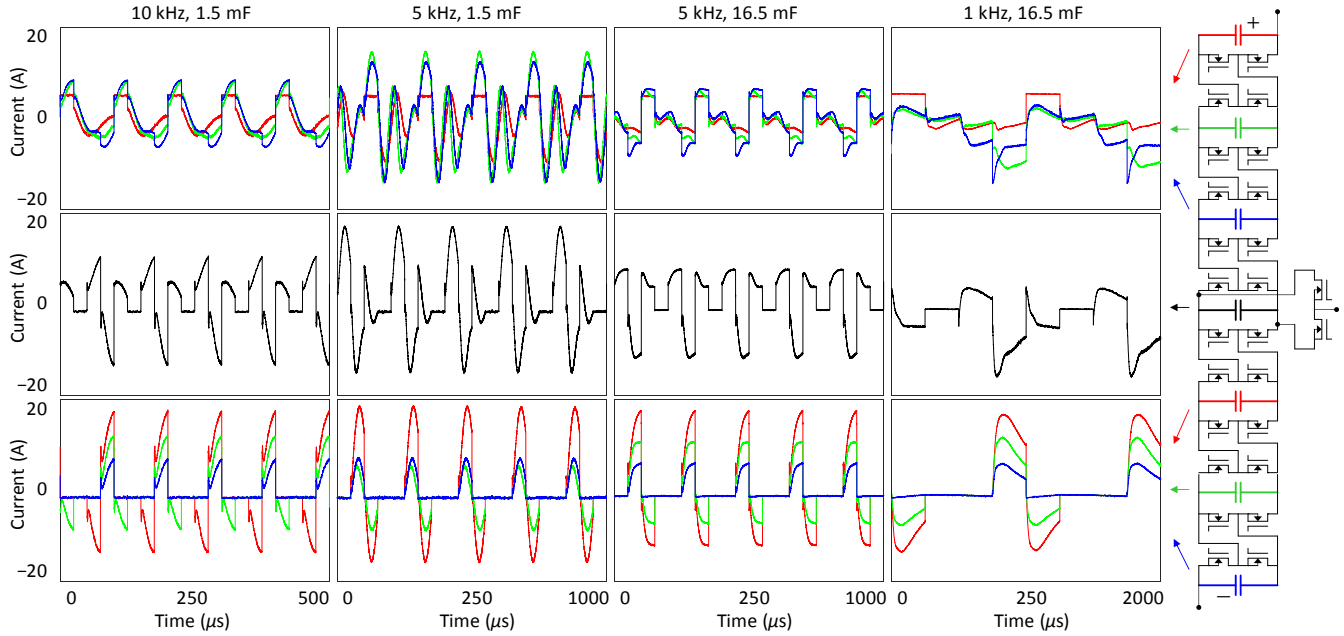

Fig. 15. Capacitor currents for various switching frequencies and module capacitances.

taken concurrently but are overlaid in the same plot. The waveforms can be overlaid because the output is dc with a fixed, repetitive switching pattern. The waveform alignments are assisted by edge-triggering the switching signals.

VI. Conclusion

This paper proposed a variant of the MMC module for wide-frequency-range operation. The proposed topology features two-terminal interconnections between the modules that allow parallel connection to cancel the oscillating power in the converter arms. The proposed solution can achieve dc output with moderate module capacitance. Compared to known methods, this solution *1)* does not impose common-mode voltages on the loads; *2)* has fewer restrictions on the maximum modulation index; *3)* fully utilizes the components at high output frequencies; and *4)* allows sensorless operation. The proposed solution is preferably used for medium-voltage motor drives, where the number of modules per arm is low.

VII. Acknowledgment

The authors thank Mr. James Evan Smith for help with the mechanical assembly of the prototype and procurement.

VIII. Appendix

A. Proof of Solution (7)

There are two possible relations between p_U and p_L:

$$\begin{cases} |p_U| > |p_L| \Leftrightarrow p_\Delta p_M V_{dc} + {p_M}^2 v_x > 0, \\ |p_U| \le |p_L| \Leftrightarrow p_\Delta p_M V_{dc} + {p_M}^2 v_x \le 0. \end{cases}$$

If $|p_U| > |p_L|$, we have $|p_U| \ge |p_\Delta|$ because

$$p_U^2 - p_\Delta^2 = \underbrace{\left(\tfrac{1}{2}V_{dc} + v_x\right)}_{\ge 0}\left[\underbrace{p_M^2\left(\tfrac{1}{2}V_{dc} - v_x\right)}_{\ge 0} + 2\underbrace{\left(p_\Delta p_M V_{dc} + p_M^2 v_x\right)}_{\ge 0}\right] \ge 0.$$

As such, $\max\{|p_U|, |p_L|, |p_M|\} \ge \max\{|p_U|, |p_M|\} \ge \max\{|p_\Delta|, |p_M|\} \ge |p_\Delta|$. All equalities are achieved simultaneously by setting $|p_M| = 0$, or $ref_M = ½ + v_x/V_{dc}$. Notice that $|p_\Delta|$ is independent of the control variable ref_M.

Alternatively, if $|p_U| \le |p_L|$, we have $|p_L| \ge |p_\Delta|$ because

$$p_L^2 - p_\Delta^2 = \underbrace{\left(\tfrac{1}{2}V_{dc} - v_x\right)}_{\ge 0}\left[\underbrace{p_M^2\left(\tfrac{1}{2}V_{dc} + v_x\right)}_{\ge 0} - 2\underbrace{\left(p_\Delta p_M V_{dc} + p_M^2 v_x\right)}_{\ge 0}\right] \ge 0.$$

Analogously, $\max\{|p_U|, |p_L|, |p_M|\} \ge \max\{|p_L|, |p_M|\} \ge \max\{|p_\Delta|, |p_M|\} \ge |p_\Delta|$. Again, by setting $|p_M| = 0$, or $ref_M = ½ + v_x/V_{dc}$, we achieve the minimum, $|p_\Delta|$.

References

[1] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *2003 IEEE Bologna Power Tech Conference Proceedings,* 2003, vol. 3, pp. 272–277.

[2] M. Glinka and R. Marquardt, "A new AC/AC-multilevel converter family applied to a single-phase converter," in *The Fifth International Conference on Power Electronics and Drive Systems, 2003. PEDS 2003.*, 2003, vol. 1, pp. 16–23.

[3] H.-J. Knaak, "Modular multilevel converters and HVDC/FACTS: A success story," *Power Electron. Appl. (EPE 2011), Proc. 2011-14th Eur. Conf.*, no. Lcc, pp. 1–6, 2011.

[4] X. Huang, Z. Wang, Z. Kong, J. Xiong, and K. Zhang, "Modular Multilevel Converter With Three-Port Power Channels for Medium-Voltage Drives," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 6, no. 3, pp. 1495–1507, Sep. 2018.

[5] M. Glinka and R. Marquardt, "A New AC/AC Multilevel Converter Family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, Jun. 2005.

[6] H. Akagi, S. Inoue, and T. Yoshii, "Control and Performance of a Transformerless Cascade PWM STATCOM With Star Configuration," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1041–1049, 2007.

[7] J. Asakura and H. Akagi, "State-of-Charge (SOC)-Balancing Control of a Battery Energy Storage System Based on a Cascade PWM Converter," *IEEE Trans. Power Electron.*, vol. 24, no. 6, pp. 1628–1636, 2009.

[8] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "A transformerless battery energy storage system based on a multilevel cascade PWM converter," in *2008 IEEE Power Electronics Specialists Conference*, 2008, pp. 4798–4804.

[9] M. Hagiwara, K. Nishimura, and H. Akagi, "A Medium-Voltage Motor Drive With a Modular Multilevel PWM Inverter," *IEEE Trans. Power Electron.*, vol. 25, no. 7, pp. 1786–1799, Jul. 2010.

[10] M. Spichartz, V. Staudt, and A. Steimel, "Modular Multilevel Converter for propulsion system of electric ships," in *2013 IEEE Electric Ship Technologies Symposium (ESTS)*, 2013, pp. 237–242.

[11] A. J. Korn, M. Winkelnkemper, and P. Steimer, "Low Output Frequency Operation of the Modular Multi-Level Converter," in *IEEE ECCE*, 2010, no. Sep., pp. 3993–3997.

[12] S. Debnath and M. Saeedifard, "Optimal control of modular multilevel converters for low-speed operation of motor drives," in *2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014*, 2014, pp. 247–254.

[13] S. P. Engel and R. W. De Doncker, "Control of the Modular Multi-Level Converter for minimized cell capacitance," *Proc. 2011 14th Eur. Conf. Power Electron. Appl.*, pp. 1–10, 2011.

[14] S. Kouro, R. Bernal, H. Miranda, C. A. Silva, and J. Rodriguez, "High-Performance Torque and Flux Control for Multilevel Inverter Fed Induction Motors," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2116–2123, Nov. 2007.

[15] R. H. Osman, "A medium-voltage drive utilizing series-cell multilevel topology for outstanding power quality," in *Conference Record of the 1999 IEEE Industry Applications Conference. Thirty-Forth IAS Annual Meeting (Cat. No.99CH36370)*, 1999, vol. 4, pp. 2662–2669.

[16] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter," *IET Power Electron.*, vol. 8, no. 3, pp. 350–360, Mar. 2015.

[17] K. Wang, Y. Li, Z. Zheng, and L. Xu, "Voltage Balancing and Fluctuation-Suppression Methods of Floating Capacitors in a New Modular Multilevel Converter," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1943–1954, May 2013.

[18] X. Shang, G. Wang, F. Li, Q. Wu, and J. Feng, "Low output frequency operation of modular multilevel matrix converter," in *2015 5th International Conference on Electric Utility Deregulation and Restructuring and Power Technologies (DRPT)*, 2015, pp. 2259–2264.

[19] M. Hagiwara, I. Hasegawa, and H. Akagi, "Start-Up and Low-Speed Operation of an Electric Motor Driven by a Modular Multilevel Cascade Inverter," *IEEE Trans. Ind. Appl.*, vol. 49, no. 4, pp. 1556–1565, Jul. 2013.

[20] M. Kamiya, "Development of Traction Drive Motors for the Toyota Hybrid System," *IEEJ Trans. Ind. Appl.*, vol. 126, no. 4, pp. 473–479, 2006.

[21] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pérez, "A Survey on Cascaded Multilevel Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[22] Y. Li, C. Wang, X. Zhao, and K. Zhang, "Research of Mining STATCOM Based on Hybrid Multilevel H-bridge Inverter," *Energy Power Eng.*, vol. 05, no. 04, pp. 636–641, 2013.

[23] J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," *IEEE Trans. Ind. Electron.*, vol. 54, no. 6, pp. 2930–2945, Dec. 2007.

[24] R. Menz and F. Opprecht, "Replacement of a wound rotor motor with an adjustable speed drive for a 1400 kW kiln exhaust gas fan," in *IEEE-IAS/PCS 2002 Cement Industry Technical Conference. Conference Record (Cat. No.02CH37282)*, 2002, pp. 85–93.

[25] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 4–17, Jan. 2015.

[26] J. Kolb, F. Kammerer, M. Gommeringer, and M. Braun, "Cascaded Control System of the Modular Multilevel Converter for Feeding Variable-Speed Drives," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 349–357, Jan. 2015.

[27] S. Debnath, J. Qin, and M. Saeedifard, "Control and Stability Analysis of Modular Multilevel Converter Under Low-Frequency Operation," *IEEE Trans. Ind. Electron.*, vol. 62, no. 9, pp. 5329–5339, Sep. 2015.

[28] A. Antonopoulos, L. Angquist, S. Norrga, K. Ilves, L. Harnefors, and H.-P. Nee, "Modular Multilevel Converter AC Motor Drives With Constant Torque From Zero to Nominal Speed," *IEEE Trans. Ind. Appl.*, vol. 50, no. 3, pp. 1982–1993, May 2014.

[29] A. J. Korn, M. Winkelnkemper, and P. Steimer, "Low output frequency operation of the Modular Multi-Level Converter," in *2010 IEEE Energy Conversion Congress and Exposition*, 2010, no. Sep., pp. 3993–3997.

[30] Jae-Jung Jung, Hak-Jun Lee, and Seung-Ki Sul, "Control Strategy for Improved Dynamic Performance of Variable-Speed Drives With Modular Multilevel Converter," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 3, no. 2, pp. 371–380, Jun. 2015.

[31] B. Li *et al.*, "An Improved Circulating Current Injection Method for Modular Multilevel Converters in Variable-Speed Drives," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7215–7225, Nov. 2016.

[32] S. Du, B. Wu, K. Tian, N. Zargari, and Z. Cheng, "An Active Cross-Connected Modular Multilevel Converter (AC-MMC) for Medium-voltage Motor Drive," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 4707–4717, 2016.

[33] S. Du, B. Wu, N. R. Zargari, and Z. Cheng, "A Flying-Capacitor Modular

Multilevel Converter for Medium-Voltage Motor Drive," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 2081–2089, Mar. 2017.

[34] M. S. Diab, A. M. Massoud, S. Ahmed, and B. W. Williams, "A Dual Modular Multilevel Converter With High-Frequency Magnetic Links Between Submodules for MV Open-End Stator Winding Machine Drives," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5142–5159, Jun. 2018.

[35] M. S. Diab, B. W. Williams, D. Holliday, A. M. Massoud, and S. Ahmed, "A modular multilevel converter with isolated energy-balancing modules for MV drives incorporating symmetrical six-phase machines," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 2715–2722.

[36] S. Du, B. Wu, and N. R. Zargari, "A Delta-Channel Modular Multilevel Converter for Zero/Low-Fundamental-Frequency Operation," *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 2227–2235, Mar. 2019.

[37] S. M. Goetz, A. V. Peterchev, and T. Weyh, "Modular Multilevel Converter With Series and Parallel Module Connectivity: Topology and Control," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 203–215, Jan. 2015.

[38] S. Du and B. Wu, "A Transformerless Bipolar Modular Multilevel DC–DC Converter With Wide Voltage Ratios," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8312–8321, Nov. 2017.

[39] M. S. Diab, A. M. Massoud, S. Ahmed, and B. W. Williams, "A Dual Modular Multilevel Converter With High-Frequency Magnetic Links Between Submodules for MV Open-End Stator Winding Machine Drives," *IEEE Trans. Power Electron.*, vol. 33, no. 6, pp. 5142–5159, Jun. 2018.

[40] M. S. Diab, B. W. Williams, D. Holliday, A. M. Massoud, and S. Ahmed, "A modular multilevel converter with isolated energy-balancing modules for MV drives incorporating symmetrical six-phase machines," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, vol. 2017–Janua, pp. 2715–2722.

[41] L. Baruschka, D. Karwatzki, M. Von Hofen, and A. Mertens, "Low-speed drive operation of the modular multilevel converter hexverter down to zero frequency," *2014 IEEE Energy Convers. Congr. Expo. ECCE 2014*, vol. 2, no. 4, pp. 5407–5414, 2014.

[42] Z. Li, A. V. Peterchev, and S. M. Goetz, "Predictive Control of Modular Multilevel Series/Parallel Converter for Battery Systems," in *Energy Conversion Congress and Exposition (ECCE), 2017 IEEE*, 2017.

[43] Z. Li, R. Lizana, A. V. Peterchev, and S. M. Goetz, "Distributed balancing control for modular multilevel series/parallel converter with capability of sensorless operation," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, no. Mmc, pp. 1787–1793.

[44] Z. Li, R. Lizana, S. Sha, Z. Yu, A. V. Peterchev, and S. Goetz, "Module Implementation and Modulation Strategy for Sensorless Balancing in Modular Multilevel Converters," *IEEE Trans. Power Electron.*, pp. 1–1, 2018.

[45] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, "Analysis and Operation of Modular Multilevel Converters With Phase-Shifted Carrier PWM," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 268–283, Jan. 2015.

[46] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*. Springer Science & Business Media, 2007.

[47] S. M. Goetz *et al.*, "Control of Modular Multilevel Converter with Parallel Connectivity—Application to Battery Systems," *IEEE Trans. Power Electron.*, vol. 32, no. 11, pp. 8381–8392, 2017.

[48] F. W. Grover, *Inductance calculations: working formulas and tables*. Courier Corporation, 2004.

[49] R. Bayerer and D. Domes, "Power circuit design for clean switching," *6th Int. Conf. Integr. Power Electron. Syst.*, no. 6, pp. 1–6, 2010.

[50] L. Muller and J. W. Kimball, "Effects of Stray Inductance on Hard-Switched Switched Capacitor Converters," *IEEE Trans. Power Electron.*, vol. 29, no. 12, pp. 6276–6280, Dec. 2014.

[51] S. Li, L. M. Tolbert, F. Wang, and F. Z. Peng, "Stray Inductance Reduction of Commutation Loop in the P-cell and N-cell-Based IGBT Phase Leg Module," *IEEE Trans. Power Electron.*, vol. 29, no. 7, pp. 3616–3624, Jul. 2014.

[52] M. C. Caponet, F. Profumo, R. W. De Doncker, and A. Tenconi, "Low stray inductance bus bar design and construction for good EMC performance in power electronic circuits," *IEEE Trans. Power Electron.*, vol. 17, no. 2, pp. 225–231, Mar. 2002.

[53] A. Dekka, B. Wu, V. Yaramasu, and N. R. Zargari, "Model Predictive Control With Common-Mode Voltage Injection for Modular Multilevel Converter," *IEEE Trans. Power Electron.*, vol. 32, no. 3, pp. 1767–1778, Mar. 2017.

[54] M. Spichartz, V. Staudt, and A. Steimel, "Analysis of the module-voltage fluctuations of the Modular Multilevel Converter at variable speed drive applications," in *2012 13th International Conference on Optimization of Electrical and Electronic Equipment (OPTIM)*, 2012, pp. 751–758.

[55] H. Fujita, S. Tominaga, and H. Akagi, "Analysis and design of a DC voltage-controlled static VAr compensator using quad-series voltage-source inverters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 4, pp. 970–978, 1996.

[56] M. Hagiwara and H. Akagi, "Control and Experiment of Pulsewidth-Modulated Modular Multilevel Converters," *IEEE Trans. Power Electron.*, vol. 24, no. 7, pp. 1737–1746, Jul. 2009.

[57] K. Li, C. Li, F. C. Lee, M. Mu, and Z. Zhao, "Precise control law of MMC and its application in reducing capacitor voltage ripple by injecting circulating current," in *2015 18th International Conference on Electrical Machines and Systems (ICEMS)*, 2015, pp. 371–377.