Two-Dimensional Molybdenum Disulfide Negative Capacitance Field-Effect Transistors

by

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Dissertation submitted in partial fulfillment of
the requirements for the degree of Doctor
of Philosophy in the Department of
Electrical and Computer Engineering in the Graduate School
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ABSTRACT

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Abstract

Essential to metal-oxide-semiconductor field-effect transistor (MOSFET) scaling is the reduction of the supply voltage to mitigate the power consumption and corresponding heat dissipation. Conventional dielectric materials are subject to the thermal limit imposed by the Boltzmann factor in the subthreshold swing, which places an absolute minimum on the supply voltage required to modulate the current. Furthermore, as technology approaches the 5 nm node, electrostatic control of a silicon channel becomes exceedingly difficult, regardless of the gating technique. This notion of "the end of silicon scaling" has rapidly increased research into more scalable channel materials as well as new methods of transistor operation. Among the many promising options are two-dimensional (2D) FETs and negative capacitance (NC) FETs. 2D-FETs make use of atomically thin semiconducting channels that have enabled demonstrated scalability beyond what silicon can offer. NC-FETs demonstrate an effective negative capacitance arising from the integration of a ferroelectric into the transistor gate stack, allowing sub-60 mV/dec switching. While both of these devices provide significant advantages, neither can accomplish the ultimate goal of a FET that is both low-voltage and scalable. However, an appropriate fusion of the 2D-FET and NC-FET into a 2D NC-FET has the potential of enabling a steep-switching device that is dimensionally scalable beyond the 5 nm technology node.

In this work, the motivation for and operation of 2D NC-FETs is presented. Experimental realization of 2D NC-FETs using 2D transition metal dichalcogenide molybdenum disulfide (MoS_2) as the channel is shown with two different ferroelectric materials: 1) the solution-processed, polymeric ferroelectric poly(vinylidene difluoride trifluoroethylene) and 2) an atomic layer deposition (ALD) grown hafnium zirconium oxide ($HfZrO_2$) ferroelectric. Each ferroelectric was integrated into the gate stack of a 2D-FET having either a top-gate (polymeric ferroelectric) or bottom-gate ($HfZrO_2$ ferroelectric) configuration. $HfZrO_2$ devices with metallic interfacial layers (between ferroelectric and dielectric) and thinner ferroelectric layers were found to reduce both the hysteresis and the threshold voltage. Detailed characterization of the devices was performed and, most significantly, the 2D NC-FETs with $HfZrO_2$ reproducibly yielded subthreshold swings well below the thermal limit with over more than four orders of magnitude in drain current modulation. $HfZrO_2$ devices without metallic interfacial layers were utilized to explore the impact of ferroelectric thickness, dielectric thickness, and dielectric composition on device performance. The impact of an interfacial metallic layer on the device operation was investigated in devices with $HfZrO_2$ and shown to be crucial at enabling sub-60 mV/dec switching and large internal voltage gains. The significance of dielectric material choice on device performance was explored and found to be a critical factor in 2D NC-FET transistor operation. These successful results pave

the way for future integration of this new device structure into existing technology markets.

Dedication

I dedicate this dissertation to my grandmother, to my friends and family, and to every person who has supported me throughout my Ph.D. The past six years have been tough, and I would not be where I am today without you all. Thank you for believing. I also dedicate this to Dusty. Thank you for being there for me, even though we are over 2500 miles apart. I am excited to finally close the gap and start our life together.

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1. Introduction and Overview

The metal-oxide semiconductor field-effect transistor (MOSFET) has revolutionized the world. As the driving technology behind the microprocessor, MOSFETs have enabled our digital world and the increasing mobility of electronics and data accessibility. However, the last ten years of MOSFET technology has revealed that these devices are rapidly approaching physical limits, primarily related to the device material (silicon) and operational mechanism. Two of the most significant factors plaguing the continued scaling (a term used to indicate the improvement in transistors by physical size reduction) of MOSFETs are operating voltage and short-channel effects. Without intervention of some type, the ability to continue scaling MOSFETs will be stalled, with impacts on the countless other technologies that have come to rely on such advancements.

The operating voltage of MOSFETs has remained pegged at ~1 V for more than a decade[1], leading to unsustainable increases in the power consumption of computer chips as more transistors are packed at smaller dimensions with each successive technology node. This obstacle of voltage scaling could be alleviated by enabling the transistor to be switched between on- and off-states with less voltage. One of the most attractive options for realizing this is the negative capacitance (NC) FET — a device that works by incorporating a ferroelectric material into the traditional MOSFET gate stack. In this configuration, the ferroelectric material acts as a step-up voltage amplifier, increasing the potential felt at the surface of the channel over the applied gate voltage.[2] This effect

has already been used to improve the subthreshold swing (SS) – the key metric for low-voltage operation – below the thermal limit with a MOSFET base.[3–6] Such an exciting result, accessible by relatively simple modification of the MOSFET structure, has led major semiconductor companies to pursue the NC-FET in earnest over the last few years.

Even if the voltage-scaling challenge should be resolved, the difficulty of physically scaling the MOSFET persists, as manifest by what are known as short-channel effects (SCEs). SCEs are deleterious effects on the operation or performance of transistors when they are scaled to dimensions that no longer allow for proper electrostatic control. The most viable option for overcoming SCEs to further scale transistors is to employ channel materials other than the traditional Si. One type of material that is especially promising is the two-dimensional (2D) transition metal dichalcogenide (TMD), which offers atomic thinness for aggressive transistor scaling.[7–12] Transistors with nominal channel lengths as small as 1 nm have been demonstrated from TMDs such as molybdenum disulfide (MoS_2)[13], showing great promise for a transistor technology that can extend to the sub-5 nm regime.

Coupling an atomically thin, 2D TMD channel with the NC-effect could produce steep switching behavior over a large range of current with a channel that is aggressively scalable. In this work, the first 2D NC-FETs have been fabricated and characterized using two different ferroelectric materials and gating configurations.

Challenges in integrating ferroelectric materials into the gate stack of 2D-FETs have been overcome while stabilizing the NC effect in these new device structures. Specifically, 2D flakes of MoS_2 were utilized as the channel with polymeric and atomic layer deposition (ALD) grown ferroelectrics. Throughout this work, several advancements were made in the field, including the removal of hysteresis, the impact of metallic interfacial layers on device performance, and the discovery of the effects of ferroelectric and oxide layer thickness on device operation. This document is organized such that each chapter represents a milestone completed while working towards the end goal of a low-voltage 2D NC-FET. The following are included:

- An introduction to next-generation transistor technology and reviews of the challenges to transistor scaling, 2D-FETs, and NC-FETs (Chapter 2).
- Review of ferroelectricity, ferroelectric materials and their use in negative capacitance FETs (Chapter 3).
- Presentation of the low-dimensional NC-FET structure that is studied in this work, with discussion of its advantages (Chapter 4).
- Presentation of the first experimentally-realized 2D NC-FET, which used a polymeric ferroelectric (Chapter 5).
- Presentation of the first CMOS compatible experimentally realized 2D NC-FET, which used an ALD-grown ferroelectric and metallic interfacial layers (Chapter 6).

- Presentation of the experimentally realized 2D NC-FET without metallic interfacial layers (Chapter 7).

2. Challenges for Future Transistors

From its invention, the market has craved the next smaller, more powerful transistor. In 1974, Robert Dennard proposed a set of rules to scale transistor dimensions while maintaining a constant electric field, known as Dennard scaling. These rules dictated MOSFET scaling for over 30 years, until around 2005, when the end of Dennard scaling marked a shift in the semiconductor industry. Continued scaling of transistor technology came at the cost of diminished performance and energy efficiency — a result of the inability to reduce the total power consumption (active and dissipated power) without decreasing transistor performance. Because the power is proportional to the square of the operating voltage, V_{DD}, the minimum power required for switching at a given performance level is dictated by the subthreshold swing (SS). The SS is a metric of the voltage required on a transistor gate in order to switch between the off- and on-states. Specifically, it is how much gate voltage must be applied to modulate the drain current by one order of magnitude, or one decade (dec) (1).[2]

$$SS = \frac{\partial V_{gs}}{\partial\,(\log_{10} I_d)} = \frac{\partial V_{gs}}{\partial \psi_s}\frac{\partial \psi_s}{\partial\,(\log_{10} I_d)} = \left(1 + \frac{C_s}{C_{ins}}\right)\left(\frac{kT}{q}\ln 10\right) \quad (1)$$

In Eqn. 1, V_{gs} is the applied gate voltage, I_d is the drain current, ψ_s is the surface potential in the semiconducting channel, C_s is the substrate capacitance, C_{ins} is the insulator capacitance, k is the Boltzmann constant, T is the temperature, and q is the elementary charge of an electron.

Conventional dielectric materials and substrates (silicon) have a positive capacitance, so the body factor (m), $1 + \frac{C_s}{C_{ins}}$, has a minimum of one. The thermal factor, $\frac{kT}{q}\ln 10$, cannot be reduced unless operating at a lower temperature. Therefore, at room temperature, the SS is thermally limited to 60 mV/dec with conventional dielectrics. The thermal limit of the SS imposes a minimum on the smallest possible V_{DD}, and thus a minimum on the power required for transistor switching. In response to this restraint, new geometries, materials, and methods of transistor operation have been introduced, some of which demonstrate improvements in sub-60 mV/dec switching by utilizing a ferroelectric incorporated into the gate stack.[14–21] A critical analysis of the progress in current, state-of-the-art transistor technology reveals many advantages of coupling the negative capacitance (NC) effect with low-dimensional transistors to overcome scaling obstacles, including the limit on the SS.

2.1 Background on Transistor Scaling

2.1.1 A Brief History

The first transistor, effectively a solid-state amplifier, was fabricated at Bell Labs in November 1947, when John Bardeen and Walter Brattain, working under William Shockley, attempted to observe variations of current in a block of germanium when a voltage was applied between the germanium and a drop of water containing electrolytes

on the germanium surface.[22,23] Seven years later, in May 1954, Gordon Teal of Texas Instruments Inc. débuted his silicon-based transistor. Silicon would prove to be a more viable material than the original germanium due to its ability to form a favorable interface with the insulating material silicon dioxide, SiO_2. In order to perform more complex tasks, the number of transistors within circuits was continuously increased. This led to the scaling down of transistors so that more could fit per unit area of a substrate. However, the increased complexity and scaling led to great concern due to the large number of components and interconnects and thus, "a tyranny of numbers" took hold.[24] By the mid-1950's, the idea of a monolithic circuit—a complete electronic circuit on a single semiconductor that would decrease the number of interconnects—gained support. Though Jack Kilby from Texas Instruments first demonstrated the monolithic concept in 1959, it was Robert Noyce from Fairchild Semiconductor who introduced the planar form of the integrated circuit in silicon, as recognized today. In Noyce's design, the metal interconnects were attached to the insulating oxide surface. In 1960, the planar integrated circuit was realized, and in 1961, the "micrologic family," an entire suite of the planar integrated circuits, was introduced to the market, leading to a new drive and desire to miniaturize.[24,25]

Over the next five years, the semiconductor industry expanded significantly. Gordon Moore recognized the potential of the integrated circuit to advance technology in a way that could deliver smaller, more powerful, and less-expensive electronics. To

get this message across to future customers and to the semiconductor industry, he published an article in *Electronics* in 1965, claiming that "[t]he complexity for minimum component costs has increased at a rate of roughly a factor of two per year…", a statement that would later become known as Moore's law.[24,26]

2.1.2 Moore's Law

Moore's law has since been revised to state that the component density of integrated circuits doubles every 18-24 months. In conjunction with Dennard Scaling, Moore's law persisted for over forty years.[27] In the last decade, however, the continued scaling of MOSFETs has slowed dramatically. Smaller transistor dimensions and stagnated operating voltages have resulted in an increased number of obstacles, including large leakage currents, increased active power, and increased delay time. New materials and geometries have been proposed to alleviate these issues, such as the FinFET[28–34]. The FinFET has shown improvements in performance when compared to the MOSFET, yet it still suffers from a non-scalable operating voltage. A different approach to combat the transistor scaling problem is to divide the solution into two parts, with the first focused on reducing the channel length required to avoid short channel effects (by lowering the screening length) and the second on lowering the supply voltage.

2.2 Screening Length

The screening length, λ, is the distance over which the potential drops at the interface of two distinct regions of a semiconductor.[35–37] In one respect, it represents the

length of the channel that is electrostatically controlled by the drain. In an energy band diagram, this is the distance over which the bands are curved between the source to channel and channel to drain (Fig. 1).

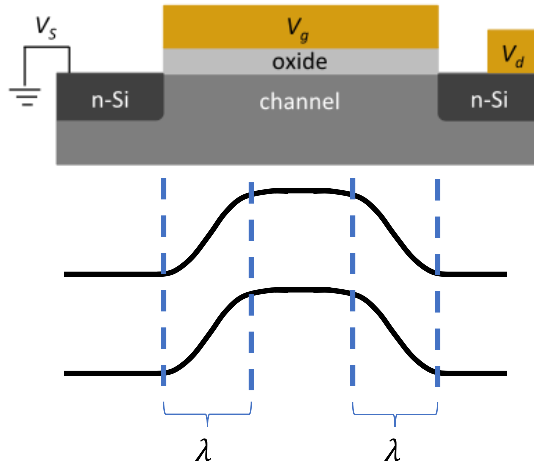

Figure 1. Transistor and energy band diagram. Top: schematic cross-sectional view of transistor (not to scale). Bottom: corresponding energy band diagram with screening length λ.

The screening length (also called the natural length) is similar to the Debye length or depletion width, and is determined by physical and electrical parameters, such as thickness and permittivity. Reductions in the screening length enable the gate to maintain electrostatic control by lowering the minimum channel length required to avoid short channel effects, which include drain induced barrier lowering (DIBL) and increased subthreshold swing. The rule of thumb for device scaling to avoid SCEs is the channel length must be at least three to six times the screening length.[38] If the channel

length is smaller than this, the drain bias can influence the surface potential in the channel and lower the source-to-channel barrier, increasing the off-current, shifting the threshold voltage, and so forth.

Because λ determines the scalability of the device, this parameter and how to minimize it should be understood. One way to accomplish this is through a simplified schematic of a MOSFET capacitance network (Fig. 2):

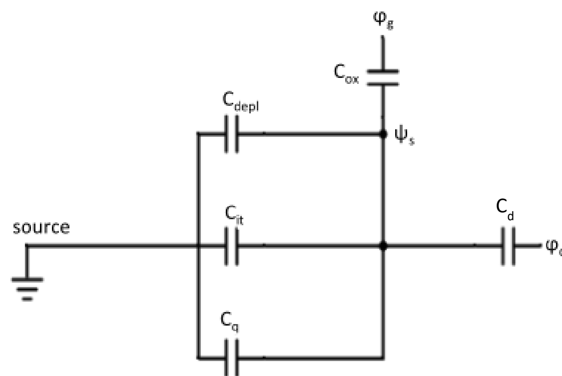

Figure 2. Simplified schematic of the capacitance network of a MOSFET. ϕ_g is the applied gate potential, ψ_s is the surface potential at the center of the channel, ϕ_d is the drain potential, C_{depl} is the depletion capacitance, C_q is the quantum capacitance, C_{it} is the interface trap capacitance, and C_d is the drain-side capacitance.

Ideally, any change in φ_g creates the same change in ψ_s, known as 1:1 band movement (2):

$$\Delta\varphi_g = \Delta\psi_s \qquad (2)$$

Realistically, the parasitic capacitances must be accounted for (3):

$$\Delta\psi_s = \frac{C_{ox}}{C_{ox}+C_{it}+C_{depl}+C_q+C_d}\Delta\varphi_g + \frac{C_d}{C_{ox}+C_{it}+C_{depl}+C_q+C_d}\Delta\varphi_d \qquad (3)$$

An oxide capacitance much greater than the drain, depletion, quantum, and interface trap capacitances ($C_{ox} \gg C_d$, C_{depl}, C_q, C_{it}) produces approximate 1:1 band movement, where $\Delta\varphi_g \approx \Delta\psi_s$. If the oxide capacitance is much less, the gate loses electrostatic control, and short-channel effects occur, including the yielding of some electrostatic control to the drain via the applied drain potential (φ_d). One way to prevent this is to reduce the screening length for a device with a scaled channel length.

The screening length is geometrically dependent and is derived from the Poisson equation for the potential profile in the semiconductor channel, from source to drain, using the appropriate boundary conditions (4).[37,39]

$$\frac{\partial^2\psi_s}{\partial x^2} + \frac{\varphi_g - \psi_s}{\lambda^2} = \frac{-\rho}{\epsilon_{body}\epsilon_{ox}} \qquad (4)$$

In eqn. 4, ρ is the charge density of the channel, ϵ_{body} is the dielectric constant of the channel, and ϵ_{ox} is the dielectric constant of the oxide. From (4), it is found that λ is dependent on the geometry of the gate.[35–37,39,40] The focus of this work will utilize the planar gate (PG) configuration, an example of which is shown in Fig. 1.

$$\lambda_{PG} = \sqrt{\frac{\epsilon_{body}}{\epsilon_{ox}} d_{body} t_{ox}} \qquad (5)$$

In (5), d_{body} is the thickness of the channel and t_{ox} is the oxide thickness. The screening length can thus be decreased through reductions in the thicknesses of the channel and the oxide, an increase in the oxide permittivity, and/or a decrease in the

body permittivity. Hence, thin channel materials and high-permittivity oxides should produce the lowest screening lengths and allow for the most aggressively scalable devices. This reasoning has led to extensive exploration of new channel materials, including two-dimensional (2D) transition metal dichalcogenides (TMDs), which are nearly atomically thin.

2.3 2D-FETs

The experimental demonstration of graphene triggered a surge of interest in 2D crystals for their novel physics and engineering properties.[12,41,42] For nanoelectronic applications, 2D TMDs have emerged among the most promising potential material, due to their semiconducting properties, crystal quality, and ease of preparation.[1,43] TMDs are composed of two elements: a transition metal (M) and a chalcogen (X), in the form MX_2.[44] Transition metals from group VI of the periodic table are used for device applications as they yield semiconducting TMDs. Chalcogens are elements in the oxygen family (excluding oxygen) and demonstrate in-plane (strong) bonding to the metal, creating a hexagonal, "honeycomb" trilayer lattice structure. Multiple layers (each with the stack of X-M-X) are held together with weak van der Waals forces. This ultimately allows TMDs to be thinned to near-atomic thicknesses through mechanical exfoliation, which is a useful technique for demonstrating 2D-FETs but not an approach that is scalable to manufacturing.

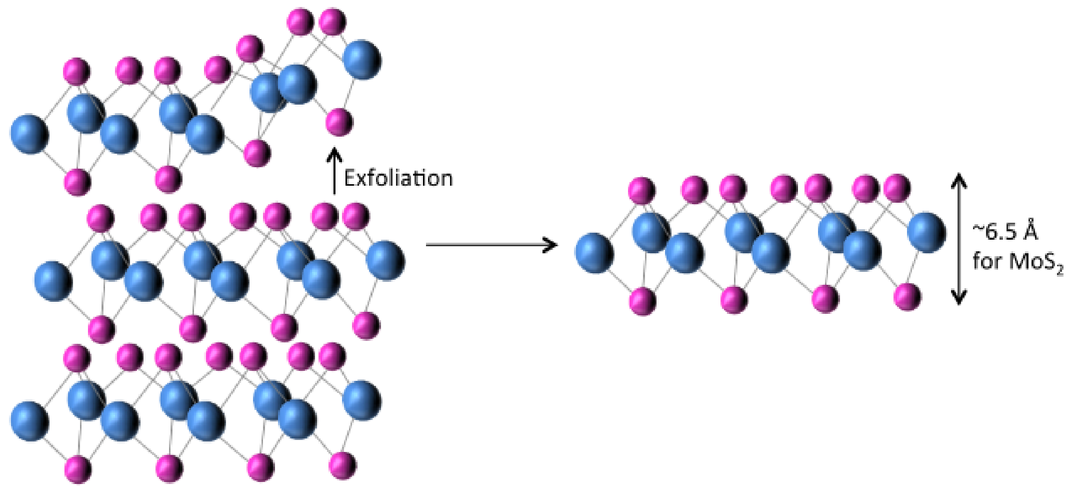

Figure 3. Exfoliation of multilayered 2D TMD. Blue spheres are the atoms of the transition metal, and purple spheres are chalcogen atoms. For molybdenum disulfide (MoS_2), each individual layer is ~6.5 Å thick.

Along with atomic-scale thickness, 2D TMDs offer pristine surfaces that lead to stable electrical and thermal characteristics. The atomic thinness allows for more aggressive scalability in 2D-FETs (without losing electrostatic control of the channel) than is possible with conventional semiconductors. Meanwhile, the pristine surface is a result of having no dangling bonds present as all are satisfied in the TMD crystal structure. This ensures no adverse reactions will occur between the channel and gate oxide or source/drain contacts and enables a uniform thickness across the material.[44–48] These benefits promise robust transistor operation by suppressing trap generation, carrier scattering, and thickness variations.

The first demonstration of FETs from TMDs used a bulk material channel in 2004.[49] Multiple types of TMDs were investigated for their use as potential channel materials, with results ranging from superconducting behavior (niobium diselenide, $NbSe_2$) to unipolar (molybdenum diselenide ($MoSe_2$), tin disulfide (SnS_2) and hafnium disulfide (HfS_2)) to ambipolar (tungsten diselenide, WSe_2). Ambipolar WSe_2 TMD-FETs were shown to operate with an ON/OFF current ratio in excess of 10^4 at a temperature of 60 K, as seen in Fig. 4(a)[49]. Further, the off-current of the device was found to be temperature dependent, as bulk conductivity of WSe_2 tends to rise with higher temperatures, reducing the ON/OFF current ratio to less than one at 300 K in Fig. 4(b)[49].

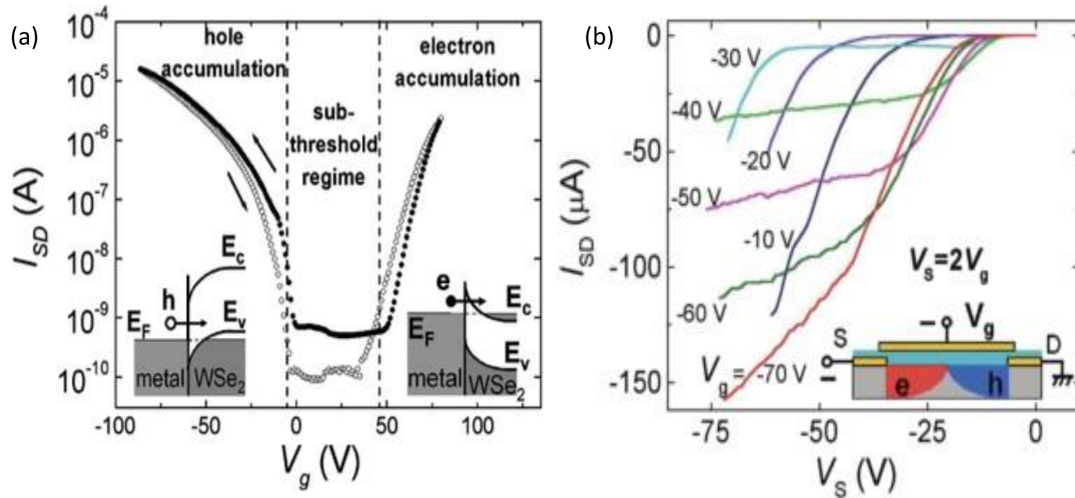

Figure 4. Ambipolar WSe_2 TMD FET operation. (a) Subthreshold hysteretic characterization with inset showing band bending under applied gate bias. (b) I_{SD} – V_g characteristics for negative values of V_g. The inset in (b) shows device structure on a bulk TMD. Fig. 4 was obtained from ref. 49.

In the fourteen years since the first demonstration, the field of 2D-FETs has seen significant advancements in terms of scaling and room temperature performance.[50–55] Recently, a 2D-FET was reported using bilayer molybdenum disulfide (MoS_2) as the channel and a carbon nanotube (CNT) gate to realize a 1 nm, ultra-short channel length with an ON/OFF current ratio of ~10^6, shown in Fig. 5.[13] The maximum on-current was ~11 μA/μm at a drain bias of 1 V, and the SS was ~65 mV/dec.

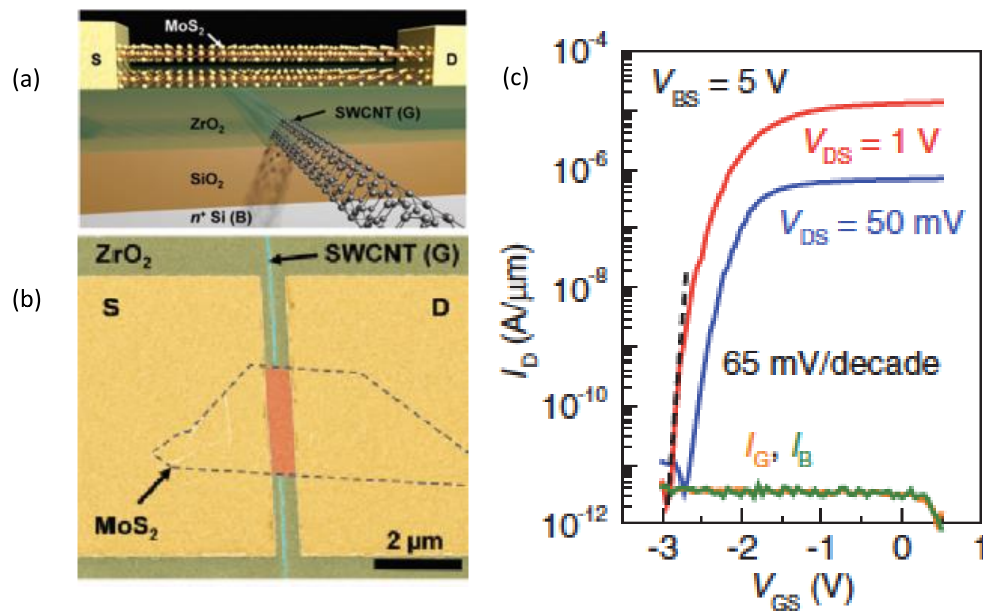

Figure 5. 2D-FET with MoS_2 channel and CNT gate. (a) Schematic of 1D 2D-FET with CNT gate and MoS_2 channel. (b) Optical image of device structure showing MoS_2 channel and CNT gate. (c) Subthreshold characteristics of 1D 2D-FET with V_{ds} of 50 mV and 1 V. This was obtained from ref. 13.

To date, the device in Fig. 5 demonstrates the smallest, electrostatically controlled channel using bilayer MoS_2, which further exemplifies the astonishing scalability provided when using 2D TMD channels.[13] However, while TMDs offer an aggressive, unmatched scalability, reducing transistor dimensions is not the only challenge for next-generation technology. As the density of transistors per chip increases, the power consumption and supply voltage become dramatically problematic and need to be addressed. These specific issues will be further discussed in the next sections.

2.4 Power Consumption and Voltage Scaling

The most efficient way to reduce the power consumption of a transistor is to scale V_{DD}, which can be accomplished in three ways: reducing the on-current (Figure 6(a)), reducing the threshold voltage (V_t) (Figure 6(b)), or reducing the SS and threshold voltage (Figure 6(c)). Diminished on-state transistor performance (reduced on-current) is not a viable option for most applications – this is actually what is done in current technologies for mobile computing applications (e.g., smartphones), where the transistors are simply operated at ~0.7 V, compromising performance for lower power and thus longer battery life. However, such reduced on-state operation isn't really solving the problem and doesn't help with the huge power draw from high-performance computing applications. The second option, to simply use a smaller V_t, results in exponentially larger off-state leakage current, which is certainly unacceptable. The only

viable option remaining is to lower the SS, which would enable V_t reduction without increase off-state leakage.

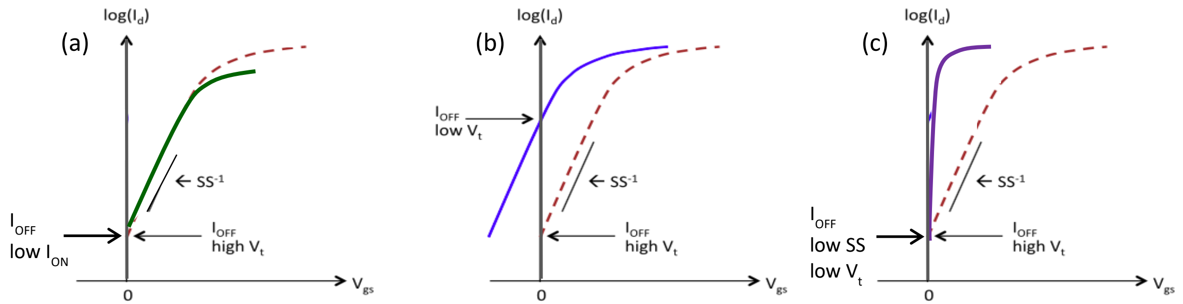

Figure 6. Impact of reducing V_{DD}. (a) Reduced I_{ON} from simply lowering V_{DD}, (b) Reduced V_{DD} with increased I_{OFF} by lowering V_t, and (c) Reduced V_{DD} by decreasing the SS. This is the only option that maintains a low I_{OFF} and a high I_{ON} while simultaneously scaling down the power consumption.

As previously stated, the subthreshold swing (SS) is a metric of how effectively the applied gate voltage can modulate the drain current, measured by the change in gate voltage required to change the drain current by one order of magnitude, or one dec, seen in eqn. 1.[2,6,15,56] With conventional dielectric materials, the body factor has a minimum of 1, since both C_s and C_{ins} are positive values, which places a limit of 60 mV/dec on the SS at room temperature and therefore limits the minimum supply voltage required for switching. The non-scalable SS has caused voltage scaling in MOSFETs to stall for over a decade, restricting both the power consumption and performance, and has resulted in a

significant uptake in research into other approaches for lowering the operating voltage. One technique that has become popular is to reduce the body factor of the SS below unity, allowing the SS to achieve sub-60 mV/dec switching at room temperature. Some of the current research in transistor technology has demonstrated sub-60 mV/dec switching by employing these methods, the most promising of which is the negative capacitance (NC) FET.[16,57–60]

2.5 Negative Capacitance FET

NC-FETs modify the traditional transduction mechanism of MOSFETs in order to bypass the thermal limit and enable lower voltage operation.[2] The negative capacitance effect is a relatively new phenomenon that enables steep, sub-60 mV/dec switching without complex geometries. NC-FETs are structurally similar to MOSFETs, with the addition of a ferroelectric material placed in series with the gate oxide. In this configuration, the ferroelectric material acts as a step-up voltage amplifier to enable sub-60 mV/dec switching.[2,3,6,14–16,20,21,57,61–68]

The NC-FET was first theorized in 2008 and has since seen a massive surge in device research.[2] The first experimental demonstration of an NC-FET occurred in the same year, using a 40 nm polymeric ferroelectric capacitor integrated into the gate stack of a MOSFET with 10 nm SiO_2.[57] Subthreshold characterization of the device included a point-by-point SS calculation to define regions of sub-60 mV/dec switching behavior. This method revealed a minimum SS of ~13 mV/dec that lasted for 10 data points and

increased afterwards to an average SS of 57 mV/dec. The hysteretic behavior of the NC-FET was found to be dependent on the drain bias and on the gate bias, with lower biases exhibiting less hysteresis. These experimental results are displayed in Fig. 7.[57]

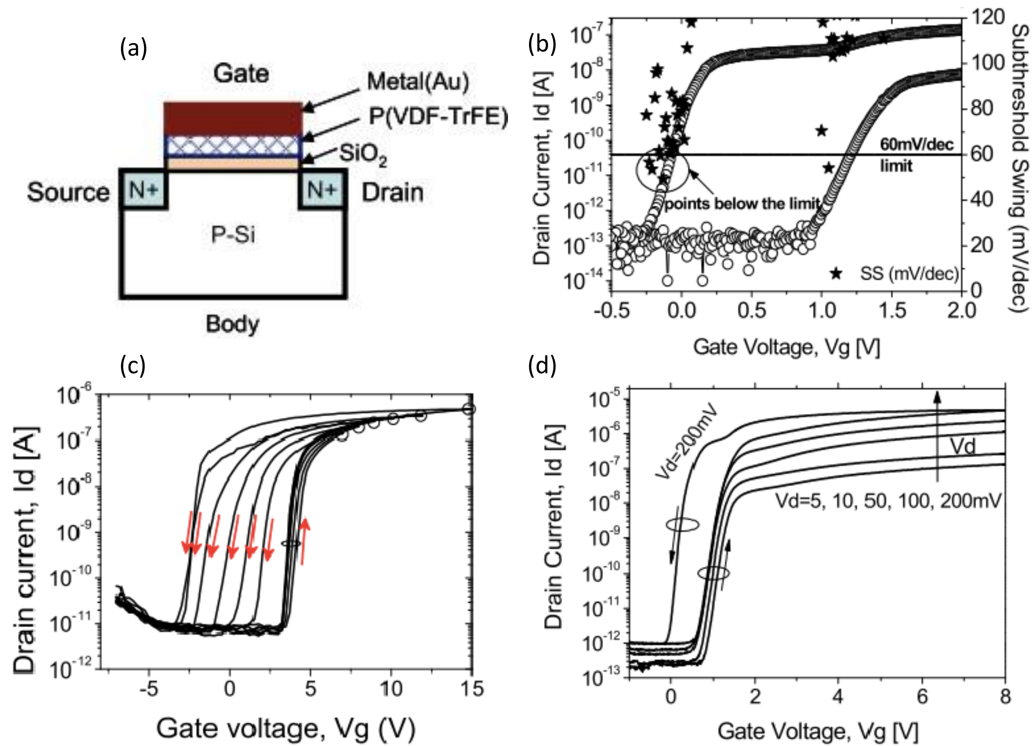

Figure 7. Performance of first experimentally realized, Si-based NC-FET. (a) Schematic of NC- FET with layers labeled (Note that the device is simply a MOSFET with the ferroelectric polymer P(VDF-TrFE) added into the gate stack). (b) Hysteretic subthreshold curve showing point-by-point SS. (c) Dependence of hysteresis on the applied gate bias. Note that the hysteresis increases with larger sweeps. (d) Hysteretic behavior with increasing drain bias. Larger drain biases lead to larger hysteretic windows. The images were obtained from ref. 57.

Despite their potential, NC-FETs using the polymeric ferroelectric did not catch on. Most other fabricated NC-FETs have used perovskite oxides as the ferroelectric, as

these materials are better understood.[6,16,18,69,70] In 2015, fully integrated NC-FETs using the ferroelectric perovskite of lead zirconium titanate (PZT) demonstrated steep on/off switching with a minimum SS of 13 mV/dec as shown in Fig. 8.[6] The voltage gain enabled by the ferroelectric material was found to increase with larger ferroelectric thicknesses, signifying a more pronounced NC effect with thicker ferroelectric layers. Unfortunately, larger ferroelectric thicknesses also increased device hysteresis, impeding low voltage operation.

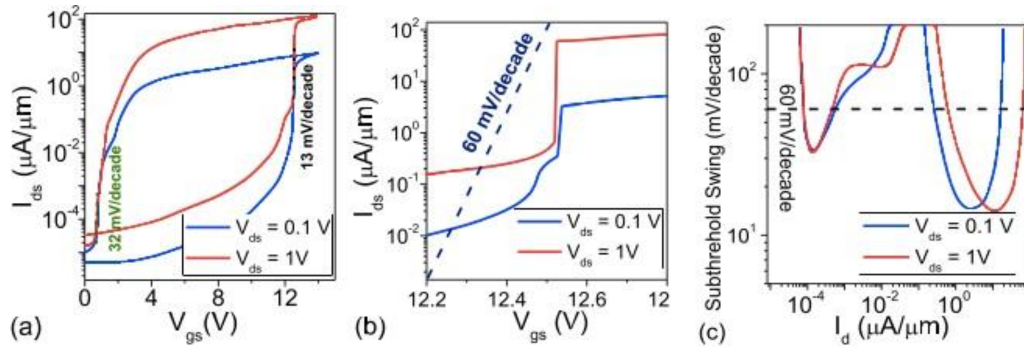

Figure 8. Si-based NC-FET operation with perovskite (PZT) ferroelectric. (a) Hysteretic subthreshold curves for different drain biases showing steep switching in both sweep directions. (b) Small region of the subthreshold curve to more closely show the sub-60 mV/dec behavior. (c) I_d ranges for sub-60 mV/dec switching. The images were obtained from ref. 6.

The significantly reduced SS capable with the NC-FETs has led to development and investigation into more scalable, non-hazardous ferroelectric materials like zirconium-doped hafnium oxides (hafnium zirconium oxide, or HZO) to incorporate

into MOSFETs and extend the life of silicon through voltage scaling.[71,72] Unlike perovskites, HZO displays extreme scalability, where thinner HZO films exhibit a larger ferroelectric response. HZO films as thin as ~1.5 nm incorporated into the gate stack of a Si FinFET have enabled effectively hysteresis-free 52 mV/dec switching, seen in Fig. 9.[20]

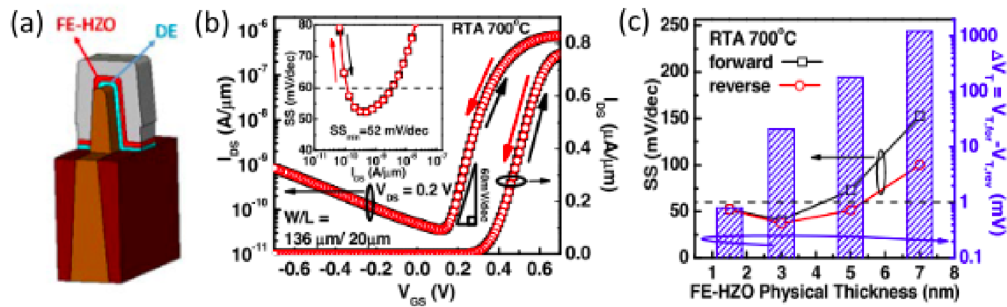

Figure 9. NC-FinFET schematics and performance. (a) Schematic and (b) subthreshold characteristics for NC-FET with ~1.5 nm HZO. (c) Subthreshold swing and hysteresis for different HZO thicknesses. Reduced hysteresis window and SS are observed with decreasing HZO thickness. These images were obtained from ref. 20.

These are just a couple of the dozens of demonstrations of Si-based NC-FETs[3,14,16,21,61,63,64,73,74] that show great promise for realizing low-voltage operation in transistors by properly incorporating a ferroelectric layer, such as HZO, into the gate stack. However, solving the voltage scaling challenge alone will not satisfy all that is needed for future technology nodes, where transistors with sub-10 nm dimensions are required in addition to operation at low voltage. Low-dimensional

materials such as 2D TMDs have been shown to yield aggressive scalability when used as the channel in FETs. Combining the NC effect with a 2D-FET – a 2D NC-FET – would allow for a steep switching device that could reduce the power consumption while continuing to be scaled. To understand how the 2D NC-FET operates, ferroelectricity and the NC effect are further discussed in Chapter 3, followed by experimental demonstration and analysis of 2D NC-FETs from MoS_2.

3. Ferroelectricity and NC-FET Operation

Ferroelectric materials are utilized almost exclusively as the gate insulator in ferroelectric FET (FeFET) memory devices. FeFETs rely on the spontaneous polarization of the ferroelectric, which generates a large corresponding hysteresis in the polarization (P) – electric field (E) characteristics, allowing for nonvolatile read/write operations.[75–81] In this configuration, the information is stored or "written" in one polarization state of the ferroelectric and "read" at the shifted threshold voltage of the polarization reversal. It wasn't until 2008, when Sayeef Salahuddin and Supriyo Datta theorized that a ferroelectric material in series with a standard dielectric would create an effective negative capacitance (NC), that these materials were considered useful for digital transistor applications.[2] Interestingly, the primary difference between an FeFET memory device and NC-FET digital transistor is that the NC-FET includes a dielectric layer in the gate stack with the ferroelectric and the FeFET does not.

The discovery of the NC effect led to the incorporation of ferroelectric materials with MOSFETs (NC-FETs) to bypass the thermal limit for switching, where NC-FETs have been shown to operate with sub-60 mV/dec SS. This chapter will provide an in-depth discussion of ferroelectricity, ferroelectric materials, and how these materials can be integrated into devices.

3.1 Introduction to Ferroelectricity

Before starting on the background of ferroelectricity, it should be noted that the term “ferroelectric” is a slight misnomer. It does not refer to the presence of iron (as the prefix “ferro” often denotes); rather, it spawns from the similar behavior of the material to the magnetic hysteresis of iron, as first described by J. Valasek in 1920.[82] Ferroelectricity was not given much thought until 1933, when I. Kurchatov gave a (now obsolete) theoretical interpretation of the phenomenon.[83] The first set of isomorphic ferroelectric crystals were produced in 1935, and with the discovery of “robust” barium titanate ($BaTiO_3$), ferroelectric materials became widely utilized as capacitors in the electronics industry. Eventually, these materials were integrated on silicon ICs as thin films and are used today in a multitude of applications including memory devices.

3.1 Polarization

The concept of polarization is crucial to understanding ferroelectricity.[84,85] For a basic understanding of polarization, consider an atom with positive nucleus and negative, spherical electron cloud. In a vacuum, the electrons will continue to orbit the nucleus within the spherical cloud. The application of an external electric force will cause the charges to separate, elongating and displacing the electric cloud so that it is no longer centered on the nucleus; thus, polarizing the atom. The same is true for a dielectric material: when placed in an electric field, the electrons of a dielectric respond

by shifting position (with respect to the nuclei) in the direction opposite the applied electric field.

The polarization of a dielectric material is mathematically expressed as a vector of the product of the vacuum permittivity (ε_0), the electric susceptibility (a measure of how easily a material will polarize in response to an applied electric field, χ_E), and the electric field.

$$\boldsymbol{P} = \epsilon_o \chi_E \boldsymbol{E} \qquad (6)$$

The electric susceptibility is related to the relative permittivity of a material.

$$\chi_E = \epsilon_r - 1 \qquad (7)$$

Conventional dielectric materials express a linear polarization (i.e. the polarization increases linearly with the applied electric field). Ferroelectric materials have a nonlinear polarization, which can be understood macroscopically through the Landau theory, discussed in *3.3.*

3.2 Crystal Structure

For a material to be considered ferroelectric, it must exhibit a nonzero spontaneous polarization arising from the atomic arrangement of ions in the unit cell of the crystal.[85,86] The presence of the spontaneous polarization implies a polar space group in the crystal structure. Ferroelectric materials are able to switch between at least two stable states of nonzero polarization with an applied electric field. One condition that ensures the existence of such discrete states of different polarization and increases the

possibility of switching between them with an applied electric field is the small, symmetry-breaking distortion of a higher-symmetry reference state that involves a polar displacement of atoms in the unit cell. Barium titanate is used as an example in Fig. 10 below, where the application of an electric field displaces the center titanium atom.

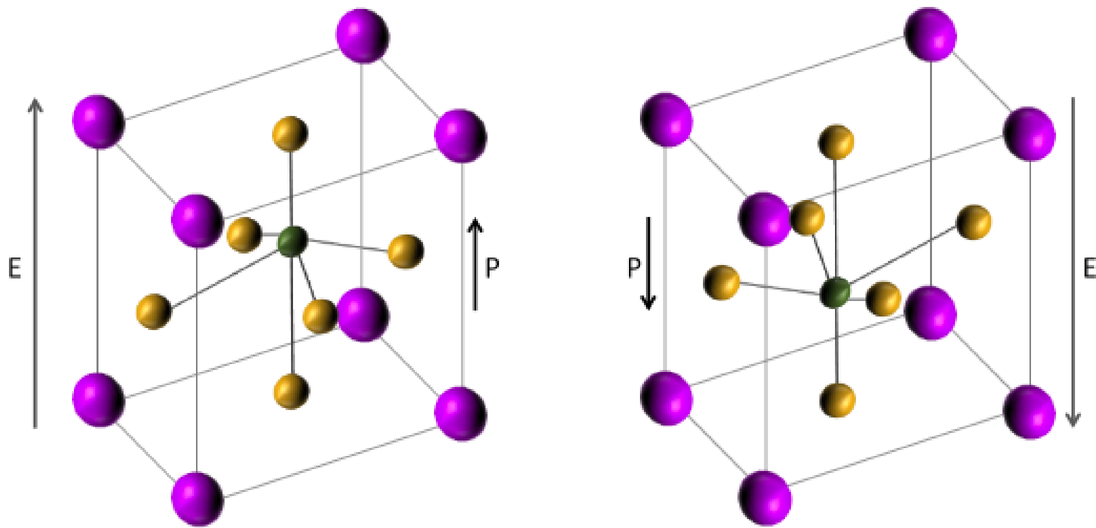

Figure 10. Unit cell crystal structure of ferroelectric barium titanate. Purple spheres are barium atoms, gold is orange, and green is titanium. The titanium atom rearranges with the applied field, polarizing the crystal.

The lack of ionic bonding in the cubic structure allows the long-range Coulomb forces to dominate over the short-range repulsions, favoring the ferroelectric state.

Most ferroelectric materials exhibit a phase transition from the ferroelectric state to the higher symmetry, nonpolar paraelectric state, usually accompanied by an increase in temperature.[85,86] The transition temperature, known as the Curie temperature (T_C), can

range from very low (1 K) to very high (above 1000 K). The symmetry breaking relationship between the ferroelectric state and the higher-order paraelectric state is consistent with the second-order transition. This will be described via the Landau theory in the following section. It should be mentioned that ferroelectric materials are not the only class of materials to have a polar space group – other materials with polar space groups are classified differently based upon the charge displacement in the crystal alone and in the presence of an applied electric field.

3.3 Landau Theory

The Landau theory describes the properties of a ferroelectric material based on symmetry considerations.[85,86] In general, it is a Taylor series expansion of the free energy of a system to describe the equilibrium behavior near a phase transition in terms of an order parameter that designates the properties of the material as continuous. This relates measurable quantities to one another using a minimum set of parameters that can be calculated from first principles or found experimentally. The Landau theory thus serves as a connection between the macroscopic behavior of a system and the microscopic models.

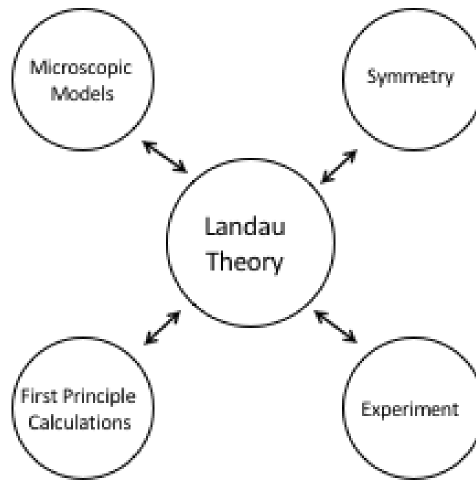

Figure 11. How the Landau theory is related to microscopic models, first principles, symmetry, and experiment.

The Landau theory assumes spatial averaging of local fluctuations, making it well suited for systems with long-range interactions, such as ferroelectrics.[85,86] The theory characterizes a transition in terms of an order parameter – a physical parameter that is zero in the high-symmetry state and becomes a finite value once the symmetry is lowered. For the case of ferroelectric materials, the free energy (*G*) of the system is described in terms of the polarization (P), where only the symmetry-compatible terms of the series expansion are retained. The state of the system is found by minimizing *G* with respect to *P*. Other thermodynamic functions can be found by differentiating *G* accordingly. This provides a straightforward, macroscopic approach to link measurable quantities near a transition.

3.3.1 Landau-Devonshire Theory

Landau's symmetry-based theory was first applied to ferroelectric materials by Devonshire, hence the Landau-Devonshire theory.[85,86] It applies a fundamental postulate of thermodynamics to describe the free energy of the ferroelectric in terms of 10 variables: three polarization (*P)* components, six stress tensor components, and one temperature (*T*) component. Ignoring the strain, the free energy of the system near the phase transition can be written as:

$$G = \frac{1}{2}aP^2 + \frac{1}{4}bP^4 + \frac{1}{6}cP^6 \qquad (8)$$

Where the coefficients a, b, and c depend on the material conditions. In this work, they are considered to be only temperature-dependent. The electric field (*E*) is then calculated with a first-order derivation of the free energy.

$$E = aP + bP^3 + cP^5 \qquad (9)$$

The Landau-Devonshire theory approach makes the following assumptions: around the Curie temperature ($T \sim T_0$):

$$a = a_0(T - T_0) \qquad (10)$$

b and c are independent of temperature, and a_0 and c are positive values. To find the energy minimum, the first derivative of the free energy is set equal to zero:

$$\frac{\partial G}{\partial P} = 0 = a_0(T - T_0)P + bP^3 + cP^5 \qquad (11)$$

A stable equilibrium exists at the polarization(s) when the second derivative of the free energy is positive:

$$\frac{\partial^2 G}{\partial P^2} = a_0(T - T_0) + 3bP^2 + 5cP^4 > 0 \ (12)$$

For simplicity, the power 4 term is now ignored. $T > T_0$ yields the trivial solution of P = 0 (no spontaneous polarization), as expected when the material becomes paraelectric. When $T < T_0$, there exist stable equilibrium at the polarization(s):

$$P_S^2 = \frac{a_0(T_0 - T)}{b} \quad (13)$$

For a second order (continuous) transition, b is assumed to be positive, as a negative b would result in a discontinuity at the Curie temperature. Using Eqn. 11, the field required to switch polarizations, the coercive field (E_c), can be found by differentiating the electric field with respect to the polarization, which is now dependent on E_c:

$$\frac{\partial E}{\partial P} = 0 = a_0(T - T_0) + 3bP^2 \ (14)$$

From here, along with Eqn. 13, the dependence of E_c on the spontaneous polarization is calculated to be:

$$P(E_C)^2 = \frac{1}{3} P_S^2 \ (15)$$

Defining the coercive field as (9) and ignoring the power 5 term:

$$E_C = aP(E_C) + bP(E_C)^3 = \frac{a}{\sqrt{3}} P_s + \frac{b}{3\sqrt{3}} {P_s}^3 \qquad (16)$$

From (13):

$$b = \frac{a_0(T_0 - T)}{{P_s}^2} \qquad (17)$$

The coercive field is then:

$$E_C = \frac{2a_0(T - T_0)}{3\sqrt{3}} P_S \approx 0.4 a_0(T - T_0) P_S \quad (18)$$

So far, the theory has ignored the presence of an external applied field. This is remedied by subtracting the energy of the coercive field from the free energy equation:

$$G = \frac{1}{2}aP^2 + \frac{1}{4}bP^4 + \frac{1}{6}cP^6 - EP \qquad (19)$$

The power 6 term is ignored for simplicity:

$$G = \frac{1}{2}aP^2 + \frac{1}{4}bP^4 - EP \qquad (20)$$

The previous conditions are applied to find the polarizations at which stable equilibrium exists. The dielectric susceptibility of the material above and below the Curie temperature can now be calculated by differentiating the free energy with respect to P and setting P = 0:

$$T > T_0 \rightarrow \chi = \frac{P}{E} = \frac{1}{a_0(T-T_0)} \qquad (21)$$

$$T < T_0 \rightarrow \chi = \frac{P}{E} = \frac{1}{2a_0(T-T_0)} \qquad (22)$$

Eqns. 21 and 22 both imply that the dielectric susceptibility disappears at $T = T_0$, causing the susceptibility to diverge. In reality, it reaches large but finite values. The second-order phase transition is demonstrated in Fig. 12.[85,86]

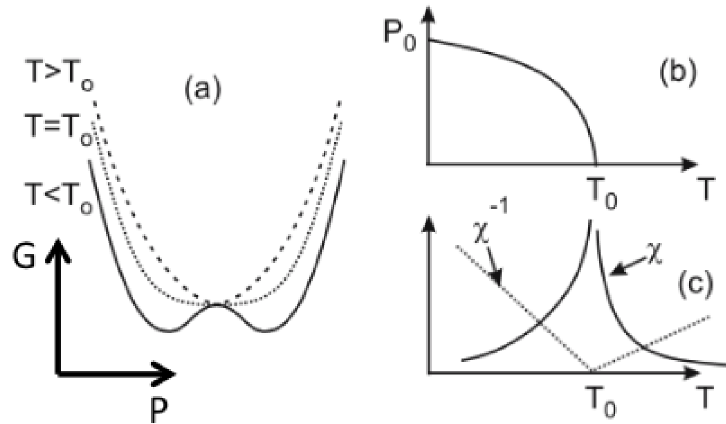

Figure 12. Second-order phase transition. (a) Temperature dependence of energy of the system. Below T_0, the energy transitions to have degenerate polarization states. (b) Spontaneous polarization as a function of temperature. Above T_0, the system transitions to the paraelectric phase with no spontaneous polarization. (c) Temperature dependence of the susceptibility (solid lines) and inverse susceptibility (dashed lines). Fig. 12 is from refs. 85 and 86.

If it is now assumed $b < 0$ (a first-order or discontinuous transition), the free energy will have a stable equilibrium at a nonzero polarization.[85,86] As the temperature is reduced, a will decrease. This causes the nonzero minimum to become lower in energy than the unpolarized state, becoming thermodynamically favorable. This temperature is T_c, which is now larger than T_0. Between T_c and T_0, the unpolarized state will occur at a local minimum of the free energy. The most important thing to note is the discontinuity at T_c, where the order parameter becomes zero. The spontaneous polarization and susceptibility can be found using the previous methods; however, the higher power terms cannot be ignored. When $T_c = T_0$, three degenerate minima of the free energy

exist simultaneously, causing the state of the system to be determined by its thermal history. This phenomenon is known as thermal hysteresis and can be found in many first-order ferroelectrics. The first-order transition is shown in Fig. 13.[85,86]

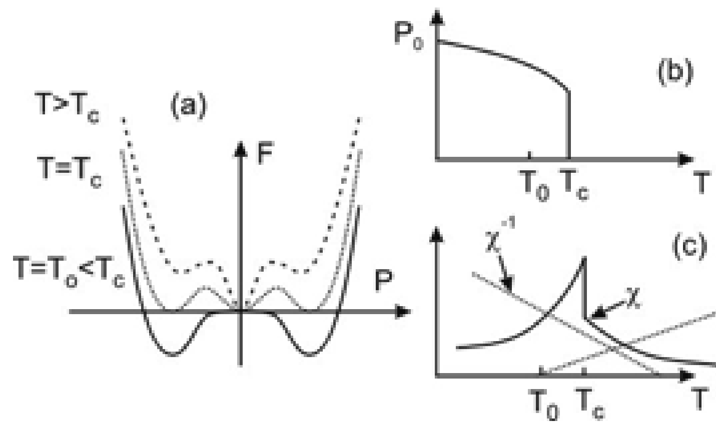

Figure 13. First-order phase transition. (a) Free energy as a function of polarization. The ferroelectric state is only favored at T < T_c. (b) Spontaneous polarization as a function of temperature. (c) Susceptibility and inverse susceptibility with temperature. Note the discontinuities in (b) and (c) at T = T_c. This is from refs. 85 and 86.

It should be mentioned that the Landau theory treats the ferroelectric as having a uniform, continuous polarization.[2,85,86] Though this is not typical, one hypothesis as

to why the Landau theory describes the behavior of ferroelectrics in this manner is the "run-away" effect.[2] Rather, any ferroelectric material that shows this effect during switching will have a "run-away" polarization, such that once one domain is

polarized, the other domains follow. This creates the positive feedback mechanism required for the NC effect to be manifest.

3.3.2 Domains

The macroscopic polarization found in the Landau theory is a result of the displacement of positive and negative charges.[85,86] To obtain the macroscopic polarization, there must be a net charge density of opposite signs on opposing sides of the structure. Any discontinuity in the net charge acts as a surface charge, increasing the energy of the system. When this occurs, the system will attempt to minimize its energy by removing the discontinuity (shielding the surface charge). In a ferroelectric thin film, the preferred orientation of the polarization is in the plane of the film, parallel to the surface, to minimize surface charges. This orientation also serves to maximize the electrostatic energy required to form domains.

Domains are regions of similar polarization and can arise for many reasons, including strain, defects, and/or the thermal or electrical history of the system.[85,86] Domains may also appear when the polarization of the film is perpendicular to the film surface. If left uncompensated, a perpendicular polarization causes an accumulation of surface charges, resulting in a depolarization field that can impede ferroelectricity. The presence of the depolarization field decreases the probability of a uniform polarization throughout the film and often results in the formation of domains.[69,87,88]

In ferroelectric thin films, the depolarization field increases with decreasing film thickness. Metal electrodes at the ferroelectric film edges provide charge compensation, reducing the depolarization field and retaining ferroelectricity. For this reason, the metal-ferroelectric-metal (MFM) capacitor is of importance, but first, we need to consider what type of ferroelectric materials are available.

3.4 Ferroelectric Materials

Since its discovery in 1920, ferroelectricity has been found to exist in a wide variety of materials.[69,79,82–84,89–91] Single crystal ferroelectrics are preferred when studying fundamental ferroelectric phenomena, as the crystallographic orientation can be controlled and the intrinsic properties more readily accessed. In electronics, single crystals are not ideal because of their high cost. Ferroelectric ceramics, however, are less expensive and can be easily processed, making ceramics the more favorable choice for many applications. However, with the continued miniaturization of technology, ferroelectric thin films have garnered the most attention. Three main categories of ferroelectric thin films have been used in NC-FETs: polymeric poly(vinylidene difluoride-trifluoroethylene) (P(VDF-TrFE)), perovskite oxides, and doped hafnia.

3.4.1 Poly(vinylidene difluoride-trifluoroethylene)

P(VDF-TrFE) is a solution-processed ferroelectric polymer that displays ferroelectric behavior in a variety of concentrations and ratios.[65,77,79,92–95] Structurally, it is composed of the monomers vinylidene difluoride and trifluoroethylene, seen in Fig. 14.

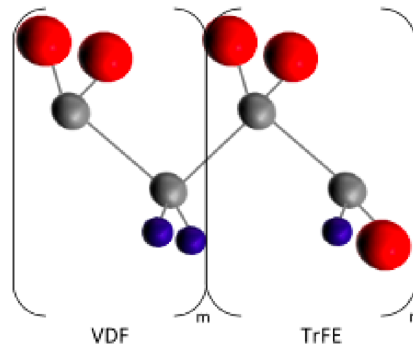

Figure 14. Structure of P(VDF-TrFE) with monomers VDF and TrFE. "m" and "n" represent the percentages of each in the polymer composition. Grey spheres are carbon atoms, red spheres are fluorine atoms, and blue spheres are hydrogen atoms.

Ferroelectricity in P(VDF-TrFE) was found to originate from the orientation of dipoles that can be reversed under an applied electric field.[94–96] Dipoles are formed due to the large electronegativity difference between the hydrogen (2.2), carbon (2.55), and fluorine (3.98) atoms. Because fluorine is much more electronegative, electrons tend to move closer to these atoms, creating a partial negative (δ-) charge on the fluorine atoms and a partial positive (δ+) charge on the hydrogen atoms.

The polymeric structure is quite complex – the carbon backbone can adapt a large number of conformations depending on the carbon-carbon bonds.[65,94–97] The linkages will adopt either the trans (T) configuration (groups bonded to the carbon atoms are on opposite sides of the carbon-carbon bond) or the gauche (G) configuration (groups bonded to the carbon atoms are on the same side of the carbon-carbon bond).

When the linkages are in the all-trans configuration (called the β-phase in PVDF), the molecule will have a zig-zag planar conformation and generate the largest polarization parallel to the carbon-fluorine dipole. This phase is stabilized by the addition of the TrFE to PVDF to produce P(VDF-TrFE) and expresses the largest ferroelectric response.

P(VDF-TrFE) is the most well studied ferroelectric polymer, in lieu of it not being CMOS process compatible. Because it is a carbon compound, P(VDF-TrFE) is easily damaged through additional processing steps. Moreover, it expresses a lower lifetime when compared to other ferroelectric thin films. The large obstacles to integration of this polymer place a limit on its usefulness in future CMOS devices.

3.4.2 Perovskite Oxides

Though not all perovskite oxides (referred to as perovskites) are ferroelectric, those that are make up the most widely studied class of ferroelectric materials.[84,91,98,99] Perovskites have the composition ABO_3, where A and B are each a cation element or a mixture of cations. The composition and cationic ordering of the crystal determine the properties.

The ideal perovskite crystal structure is the higher symmetry reference state that produces the paraelectric phase.[84,91,98,99] It is a simple cubic lattice, where an “A” cation is located at each corner, a “B” cation in the center, and an oxygen atom at the midpoint of each edge. The susceptibility of the reference state to distortions, such as the displacement of the center atom in the ferroelectric state, relates to the structural tension

of the cubic crystal as an ionic solid. The higher symmetry state will be stable if these rules are followed: a cation is surrounded by as many anions as can touch it, but no more, and all anions must touch cations where the distance between them is determined by the sum of their atomic radii. When these are satisfied, the ideal structure is maintained. Deviations can result in a small, polar displacement, like in ferroelectric barium titanite ($BaTiO_3$) in Fig. 12.

$BaTiO_3$ has four different stable states, each one occurring in a different temperature range.[100] Above 393 K, the ideal paraelectric cubic structure is observed. From 393 K to 278 K, it transforms from the cubic to the ferroelectric tetragonal phase through a small displacement of the titanium atom and the accompanying strain. At 278 K, it transitions to the ferroelectric orthorhombic phase, and finally to the rhombohedral phase at 183 K. The transition temperatures can be reduced by the application of an external stress on the system. The four states of $BaTiO_3$ are closely related to structures of lead zirconium titanate (PZT) and other +2/+4 cation perovskites.

PZT is the most relevant of the perovskite oxides and is used in many different electronic applications, despite the low Si-compatibility.[70,91,101] Additionally, PZT suffers from increased processing difficulties, lead-related environmental issues, increasing ferroelectricity with larger thicknesses, and small bandgaps. The shortcomings of PZT have set a limit on the scalability of ferroelectric devices, amplifying research into non-perovskite ferroelectrics.

3.4.3 Doped Hafnium Oxides

Doped hafnium oxide thin films are simple, binary oxides with a non-perovskite crystal structure and relatively low permittivities that can be grown using CMOS-compatible atomic layer deposition (ALD) processes.[68,71,72,89,102–107] Ferroelectricity has been demonstrated with a variety of dopants, such as silicon, yttrium, aluminum, and zirconium. Zr-doped HfO_2 films ($HfZrO_2$ or HZO) are favored for integration into CMOS technology for chemical and physical similarities to HfO_2 and relatively low crystallization temperatures.

Ferroelectricity in HZO stems from a size-driven tetragonal to orthorhombic phase transition.[71,108] As deposited, HZO thin films demonstrate a linear polarization vs. electric field (P-E) response due to the tetragonal phase of the crystal structure. To realize ferroelectricity, the nonpolar tetragonal and monoclinic (high temperature) phases need to be suppressed during crystallization. Confinement of the films by titanium or tantalum nitride (TiN or TaN, respectively) metallic electrodes can aid in this process, increasing the stability of the ferroelectric orthorhombic phase.

HZO exhibits an inverse scaling behavior of polarization versus thickness compared to conventional perovskite ferroelectrics, where the remnant polarization observed in a 10 nm HZO thin film requires PZT thicknesses of more than 100 nm.[71,108,109] Additionally, ferroelectricity has been demonstrated in HZO films less than 2 nm thick.[20] Integration of such thin films into a device structure typically presents the possibility of

leakage current issues. Thin HZO films avoid this problem, thanks to the strong bonding between the oxygen and the hafnium and zirconium atoms. In all, HZO presents as a promising solution for integrating scaled ferroelectric materials into future electronic applications.

3.5 Ferroelectric Capacitors

The simplest description of the behavior of a ferroelectric material is through a metal-ferroelectric-metal (MFM) capacitor. In a conventional parallel-plate dielectric capacitor, applying a voltage at one terminal causes the material to polarize, and the positive and negative charges of the dielectric separate such that the amount of separated charge (polarization) increases linearly with increasing applied voltage.[67,84,110] Ferroelectric materials differ from conventional dielectrics in that they exhibit a nonlinear polarization, where a small change in applied voltage can produce an enormous change in the polarization.

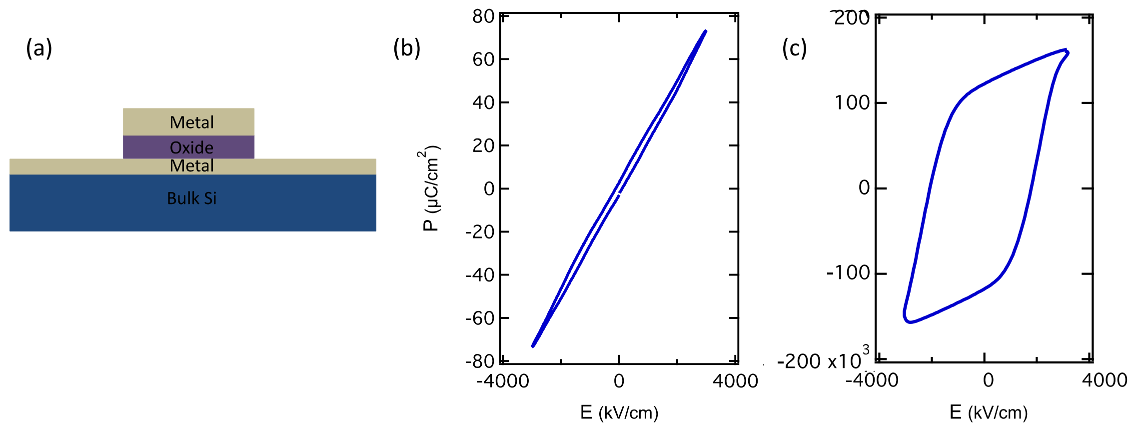

Figure 15. Polarization – electric field curves of a metal-oxide-metal capacitor. Capacitor schematic is shown in (a) with P-E curves from (b) a normal dielectric material and (c) a ferroelectric material. Note the non-linear polarization of the ferroelectric with a small change in the applied field.

Once a voltage has been applied, the ferroelectric material exhibits a spontaneous polarization that is reversible above a threshold voltage (coercive voltage), resulting in an accumulation of bound "ferroelectric" charge at the material surface.[67,84,110] The "ferroelectric" charge can exceed the charge supplied by the electrodes and can continue to increase as the applied voltage decreases. Because the capacitance of the system is defined as the charge per voltage, an increase in charge with a reduction in voltage produces a negative differential capacitance. This has been simulated with each of the ferroelectric materials discussed in Section 3.4.[2,3,19,62]

3.6 Negative Capacitance FETs

As previously shown in Eqn. 1, the SS is thermally limited to 60 mV/dec by the Boltzmann factor when using a conventional dielectric in the gate stack. Because the dielectric capacitance and the substrate capacitance are both positive, the body factor has a minimum of one, and the SS a minimum of 60 mV/dec. In 2008, it was theorized that incorporating a ferroelectric material in series with the gate oxide would result in an effective negative capacitance in the gate stack.[2] This stems from the negative slope of the polarization – electric field (P-E) characteristics (a scaled version of the charge – voltage (Q-V) characteristics) around the origin. The capacitance is defined as the charge per voltage ($\frac{Q}{V}$), so a negative slope of the P-E curve identifies a region of effective negative capacitance.[6,110] Replacing the positive insulator capacitance in Eqn. 1 with the negative capacitance (replacing the gate oxide with a ferroelectric material) would result in a body factor less than one and sub-60 mV/dec switching.

The negative capacitance region of the ferroelectric polarization is inherently unstable.[2,110] As was explained in Section 3.3, the free energy, U, of a ferroelectric material can be developed in terms of the polarization, which has a minimum of two stable degenerate states.[84,85] The energy of the ferroelectric is related to the capacitance by (21)[110]:

$$C = \left(\frac{d^2G}{dP^2}\right)^{-1} \qquad (21)$$

Therefore, the capacitance is negative in regions where the free energy profile is concave, shown in Fig. 16.

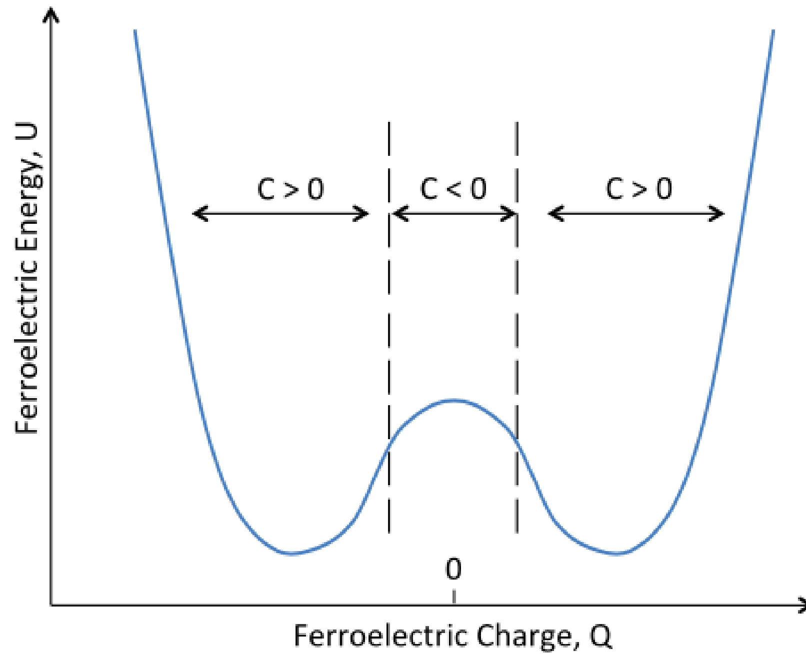

Figure 16. Energy landscape (U) of a ferroelectric capacitor without an applied voltage. The capacitance is negative only between the stable polarization states, around the region where $Q_F = 0$.

Though inherently unstable, the NC-effect can be stabilized by placing it in series with a conventional dielectric.[2,67,110] In this configuration, the ferroelectric acts as a step-up voltage transformer. Voltage amplification has been observed and measured in NC-FETs, where the voltage at the interface between the ferroelectric and the dielectric is

amplified over the applied gate voltage.[2,5,6,16,21] This behavior is understood by looking at the sum of the voltages across the ferroelectric and the dielectric (23).[6]

$$V_{gs} = V_{Fe} + V_{int} \quad (23)$$

In Eqn. 23, V_{Fe} is the voltage across the ferroelectric material and V_{int} is the internal voltage between the ferroelectric and the oxide. It was previously established that there is an unstable region of negative slope in the P-E characteristics of a ferroelectric, which can also be interpreted as a region of negative differential voltage. Because the voltage across the ferroelectric is negative, the voltage across the dielectric must be larger than that applied.

Direct experimental observation of the negative capacitance regime in the P-E characteristics was thought impossible because of hysteretic jumps, until 2014.[110] In this experiment, a 60 nm lead zirconium titanate (PZT) ferroelectric capacitor was placed in series with a 50 kΩ resistor (R) and an AC voltage pulse was applied. The calculated polarization plotted as a function of voltage experimentally demonstrated small regions of increasing polarization with decreasing voltage, or negative capacitance, seen in Fig. 17.[110]

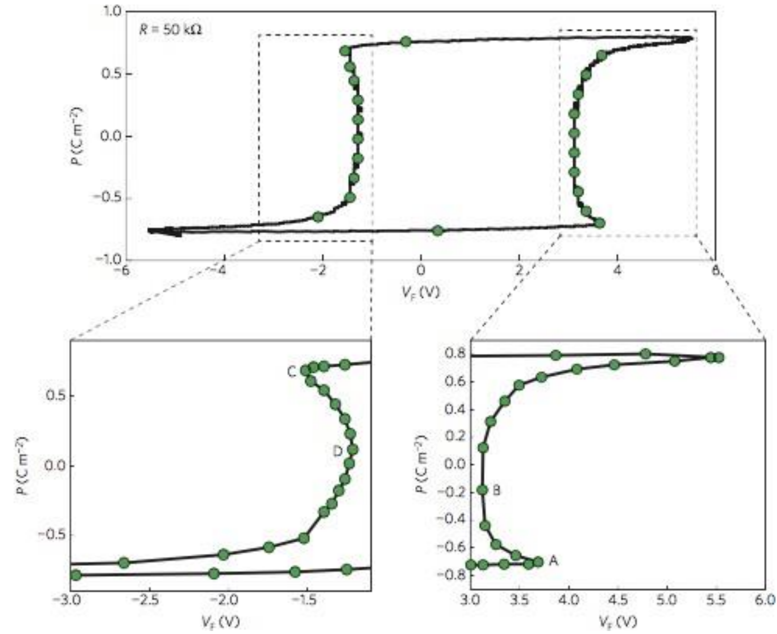

Figure 17. Ferroelectric polarization as a function of voltage, showing experimental evidence of negative capacitance. The insets show regions where the voltage and the polarization are of opposite polarity. Figure 16 is from ref. 110.

The NC effect has been successfully applied in Si-based NC-FETs with a variety of ferroelectric materials (discussed in Section 3.4) to achieve internal voltage amplification and steep switching well below 60 mV/dec.[14,20,61–64,69,111,112] Further, the NC effect has been demonstrated in highly scaled FinFETs, which report SS as low as 8.5 mV/dec over eight decades of drain current, shown in Fig. 18.[16,18] The key performance metrics of several of the best NC-FETs to date are outlined in Table 1.

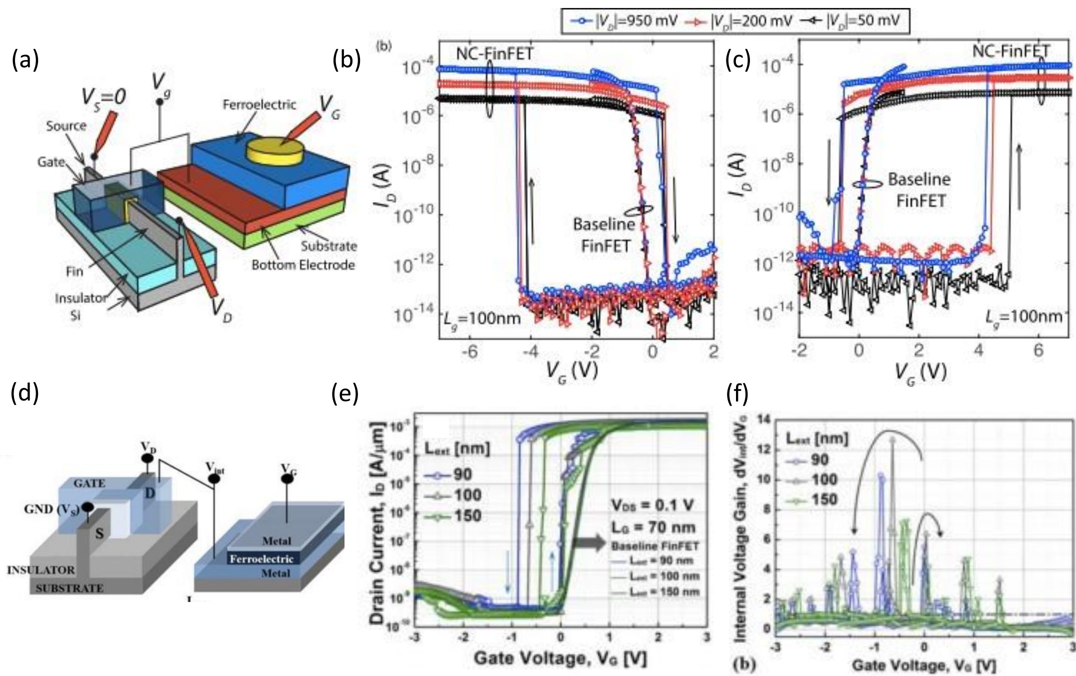

Figure 18. Negative Capacitance FinFETs. Top: (a) NC-FinFET schematic with ferroelectric capacitor externally connected. (b, c) Hysteretic subthreshold comparison of baseline (b) p-type and (c) n-type FinFET to NC-FinFET. (bottom) Sub-20 current NC-finFET (d) Schematic of a second NC-FinFET with ferroelectric capacitor externally connected. (e) Hysteretic subthreshold characterization of NC-FinFETs with different channel lengths. (f) Internal voltage gains for different channel lengths. (a-c) Are from ref.16, (d-e) are from ref. 18.

Table 1. Key performance metrics for NC-FET operation.

MOS Structure	Ferroelectric	Thickness	Average SS	Hysteresis	Reference
Planar	P(VDF-TrFE)	40	~ 13 mV/dec	Yes	4
Planar	P(VDF-TrFE)	16	~ 45 mV/dec	No	14
Fin	PZT	60	~ 12 mV/dec	Yes	16
Planar	PZT	100	~ 13 mV/dec	Yes	6
Planar	HZO	1.5	~ 52 mV/dec	No	20

Understanding and development of the theory and materials related to ferroelectricity has made exploration of NC-FETs possible. It was less than a decade ago that HZO ferroelectric thin films were discovered, and now they have already been demonstrated as part of the gate stack of an aggressively scaled NC-FinFET technology. The remarkable progress in NC-FET performance has the potential to extend the life of silicon in the semiconductor industry. However, as transistor technology shrinks towards the 5 nm node, maintaining electrostatic control of the channel becomes exceedingly difficult, regardless of the gating effect. As previously stated, one such way to bring longer life to transistor technology is to combine an aggressively scalable channel material, such as the transition metal dichalcogenide, with the NC effect to accomplish the ultimate goal of a low-voltage and dimensionally scalable transistor.

4. Overview of 2D NC-FET Device Approach

The reviews of the state-of-the-art transistors and ferroelectric materials in Chapters 2 and 3, respectively, have revealed several aspects that must be addressed for future transistor technology. To reduce the heat generated, the supply voltage must be lowered. In an NC-FET, a ferroelectric material placed in series with the gate oxide of a FET effectively acts as a step-up voltage transducer, amplifying the internal voltage over that applied to the gate, thus enabling a reduction in the required supply voltage. Future transistors also require dimensional scalability; though the ferroelectric can lower the supply voltage, it cannot improve the size scalability of silicon. This chapter will overview how ferroelectric materials integrated into the gate stack of 2D-FETs provides an elegant, combined solution to these obstacles. What's more, this solution provides further advantages beyond the combination of two devices, such as the less variable substrate capacitance of the 2D material helping to stabilize the NC effect. The detailed fabrication processes are presented in Chapters 5-7, while an outline of the device structure and the projected performance is presented here.

4.1 2D NC-FET Device Structure

At the most basic level, the 2D NC-FET consists of a ferroelectric capacitor in series with a 2D-FET. Fig. 19 provides a general schematic of a 2D NC-FET (note Figure 19 is not to scale) with integrated ferroelectric. Though there are a few options for the gating configuration of the 2D NC-FET, the gating scheme is a simplified bottom-gate in

this schematic. Metal source (S) and drain (D) contacts are Ni and a high-*k* dielectric is employed as the gate oxide.

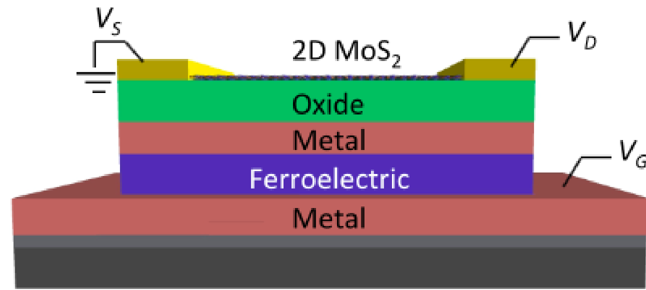

Figure 19. Schematic cross-section of a 2D NC-FET (not to scale). Note the 2D-FET is in series with an MFM capacitor, where the top metal of the capacitor serves as the traditional 2D-FET gate.

4.2 Advantages of the 2D NC-FET

Though silicon offers a more controlled and established device fabrication, the disadvantages associated with further silicon scaling warrant a consideration of new channel materials. The 2D NC-FET allows for extreme scalability because of the atomic thinness of 2D TMDs. With the assumptions of a monolayer of MoS_2 for the semiconductor channel (d_{body} = 0.65 nm, ε_{body} = 3.3), a planar gate configuration, and high-*k* dielectric HfO_2 (ε_{ox} = 30), the screening length can be scaled to $\approx 0.267\sqrt{t_{ox}}$. Therefore, for a 2D-FET with 10 nm HfO_2, the screening length is ~0.855 nm, and, to avoid short channel effects, the gate/channel length must be a minimum of ~4.227 nm.

Comparatively, for a silicon channel, the minimum channel thickness before experiencing quantum confinement effects is ~8 nm. Using the planar device structure with a channel thickness of 8 nm and ε_{body} = 11.7, the screening length is ~5.586 nm, and the gate length has a minimum of 27.928 nm. Realistically, a silicon channel will be thicker than 8 nm, increasing the screening length and further limiting the scaling of such devices.

A 2D channel offers a more stable substrate capacitance than silicon, stemming from the lack of mobile charges and ions within the structure, along with the material's thinness. A more stable C_s leads to better capacitance matching with the network of C_{Fe} and C_{ox}, to enable reproducible access to the negative capacitance operating regime. This should mean a more stable sub-60 mV/dec switching behavior, and thus the achievement of consistent low-voltage switching.

Additionally, the 2D channel materials, such as TMDs, open the way for a great variety of integration approaches. For instance, TMDs are van der Waals layered so that they are not actually bound to any particular substrate. This makes it possible to integrate the 2D NC-FET on substrates other than the traditional silicon. A further advantage of this substrate independence is in the ability of stacking the 2D materials to form ultrathin interfaces, such as with hexagonal boron nitride (h-BN) as a gate dielectric directly interfacing with the TMD channel.[113] Also, there is an increasing

variety of 2D semiconducting material options, both among the TMD family and also in other families, such as the X-enes (e.g., phosphorene, germanene).[9,12,19,42]

The advantages are many and varied for the 2D NC-FET device. From dimensional scalability and the potential for low-voltage operation to customizability with other stacked 2D layers and substrates, there is much that can be gained from 2D NC-FETs. The first step toward realizing such promises is to experimentally demonstrate these devices and characterize their behavior.

5. 2D NC-FET with P(VDF-TrFE)

5.1 Overview

As pointed out in previous chapters, the continued scaling of transistor technology has led to the need for a low-voltage device. Introduction of a ferroelectric material in series with the gate oxide of Si-based MOSFETs has produced steep switching in the form of NC-FETs.[3,5,6,14,57] This chapter is focused on the first experimental demonstration of the 2D NC-FET, using MoS_2 as the 2D channel material along with ferroelectric copolymer poly(vinylidene difluoride-trifluoroethylene), P(VDF-TrFE). The ferroelectric behavior of the P(VDF-TrFE) in a 70:30 ratio is characterized by fabricating a 0.09 mm^2 capacitor with a 3% (w/w) P(VDF-TrFE) in methyl ethyl ketone (MEK). This P(VDF- TrFE) is then integrated into the gate stack of top-gated MoS_2 FETs in two configurations: 1) with an internal gate metal separating the P(VDF-TrFE) and gate dielectric and 2) without such an internal gate metal layer. It is found that the internal metal layer is critical for reducing interfacial effects that mitigate the NC effect. The 2D NC-FET without the interfacial layer demonstrated an ~50% reduction in the SS when compared to the original 2D-FET yet was unable to achieve sub-60 mV/dec operation. When the interfacial layer was present, steep switching was demonstrated with a minimum SS of 11.7 mV/dec over three decades.

5.2 Experimental Details

5.2.1 3% P(VDF-TrFE) capacitors

Capacitors were initially fabricated to study the response of the ferroelectric. The bottom electrodes were designed in KLayout, a CAD software design suite. Poly(methyl methacrylate) (PMMA) 950 A3 was spin-coated on a p++ silicon wafer with 10 nm thermally grown oxide at 500 rpm for 5 s then 4000 rpm for 60 s and baked at 180°C for 180 s. The electrode pattern was written using electron beam lithography (EBL) in a 600 μm field of view with 60,000 exposure points. The electron beam was set to a 2 nA current with an exposure of 0.45 μs to create a dose of ~1145 $\mu C/cm^2$. The pattern was developed in a 3:1 ratio of isopropyl alcohol (IPA) to methyl isobutyl ketone (MIBK) for 120 s, rinsed with IPA, and dried with nitrogen gas. The electrode pattern was metallized employing an electron beam evaporator with 5 nm Ti, 30 nm Au. Lift-off was performed in a beaker of acetone heated to 80°C for ~5 minutes. The wafer was rinsed with IPA and dried under nitrogen gas.

P(VDF-TrFE) was purchased in a 70:30 ratio. A 3% (w/w) solution of P(VDF-TrFE) in methyl ethyl ketone (MEK) was spin-coated over the bottom electrodes at 500 rpm for 5 s then 3000 rpm for 30 s followed by heating at 150°C for 600 s. Top electrodes were fabricated using a shadow hard mask and metallized via electron beam evaporation with 50 nm Au. The capacitors were sent to Radiant Technologies© for

initial P-E characterization using a ferroelectric tester unit. Eventually, such a system was acquired so that the P-E characterization could be performed in-house.

5.2.2 MoS_2 2D-FET Fabrication

Alignment marks were designed in KLayout and fabricated using the same procedure for EBL patterning as described in subsection 5.2.1. The pattern was developed in a 3:1 ratio of IPA to MIBK for 120 s, rinsed with IPA, and dried with nitrogen gas. The alignment pattern was metallized using an electron beam evaporator with 5 nm Ti, 30 nm Au. Lift-off was performed in a beaker of acetone heated to 80°C for ~5 minutes. The wafer was rinsed with IPA and dried under nitrogen gas.

MoS_2 was mechanically exfoliated over the alignment mark pattern. The thicknesses of the MoS_2 flakes were optically characterized and confirmed with atomic force microscopy (AFM). MoS_2 flakes with thicknesses ~8-10 nm were selected for device fabrication based on previous reports of this being an optimal thickness range for 2D-FET performance.[7,8,114] The contacts, leads, and source/drain pads for substrate-gated MoS_2 2D-FETs were designed in KLayout. The same PMMA/EBL/development process previously described was employed to write the contacts and leads in the same step. Once written and developed, the contacts and leads were metallized with 40 nm Ni. Lift-off was performed in a beaker of acetone heated to 80°C for ~15 minutes. The wafer was rinsed with IPA and dried under nitrogen gas. The PMMA/EBL/development process was again repeated to create the S/D pads, followed by metallization using an electron

beam evaporator with 2 nm Ti/20 nm Pd/35 nm Au. Lift-off was performed in a beaker of acetone heated to 80°C for ~5 minutes. The substrate-gated MoS_2 FETs were electrically characterized with an Agilent (Keysight Technologies) B1500A Semiconductor Parameter Analyzer.

5.2.3 2D NC-FET Fabrication

A 10 nm (125 cycles) aluminum oxide (Al_2O_3) gate oxide layer was grown via a custom-built Kurt J. Lesker plasma-enhanced ALD cluster system over the MoS_2-FETs. The Al_2O_3 precursors were trimethyl aluminum (TMA) and water vapor (H_2O). The system was set to at 120°C with a pressure of ~1.2 Torr. An ambient Ar gas was flowing throughout deposition. The pulse/purge rates for the TMA/H_2O cycles were 40 ms/20 s/140 ms/20 s.

5.2.3.1 Without Interfacial Metal Electrode

A 1% (w/w) solution of P(VDF-TrFE) in MEK was spin-coated over the Al_2O_3 at 500 rpm for 5 s, then 3000 rpm for 30 s, followed by baking at 150°C for 600 s. A top gate was established using a shadow hard mask placed directly over the P(VDF-TrFE) and metallized with electron beam evaporation of 50 nm Au. The 2D NC-FETs without an interfacial metal layer between the P(VDF-TrFE) and the Al_2O_3 were electrically characterized. The device cross-structure is shown in Fig. 20(d).

5.2.3.2 With Interfacial Metal Electrode

On a separate wafer with back-gated MoS_2 2D-FETs and 10 nm ALD-grown Al_2O_3, an interfacial metal electrode was designed with KLayout and fabricated using the same PMMA/EBL/development process as before. The interfacial electrode was metallized using an electron beam evaporator and 50 nm Au, and electrically characterized as a top-gate for comparison purposes. A 1% (w/w) solution of P(VDF-TrFE) in MEK was then spin-coated over the interfacial layer at 500 rpm for 5 s, then 3000 rpm for 30 s, followed by baking at 150°C for 600 s. A top gate was established using a shadow hard mask and metallized with electron beam evaporation of 50 nm Au. These 2D NC-FETs with an interfacial metal layer between the P(VDF-TrFE) and the Al_2O_3 were then electrically characterized. The device cross-structure is shown in Fig. 20(e).

5.3 Results and Discussion

It should be noted that the change in concentration of the P(VDF-TrFE) from the capacitors to inclusion in the 2D NC-FET was a result of the excessively large voltage required to observe the full P-E behavior, seen in Fig. 20(a).

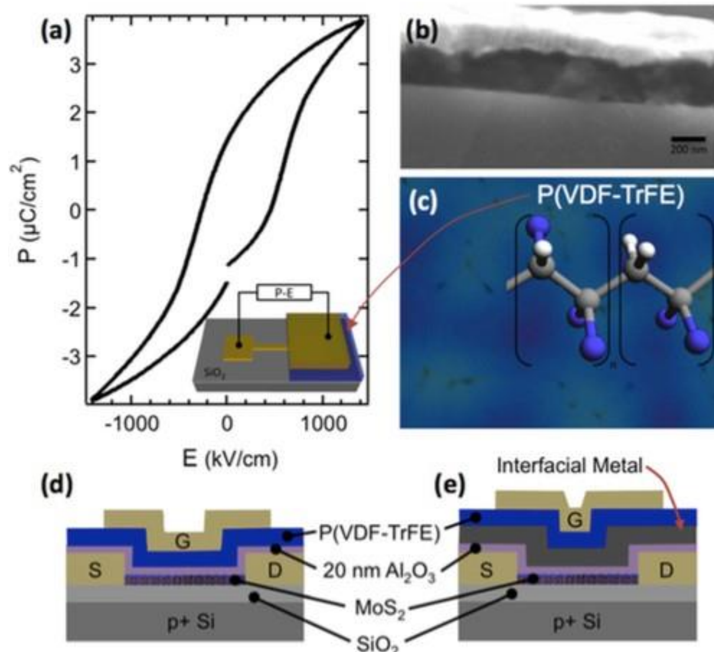

Figure 20. Ferroelectric polymer P(VDF-TrFE) and its integration into a 2D NC-FET. (a) Polarization vs. electric field curve for a 3% (w/w) P(VDF-TrFE) capacitor with the inset showing schematic of the capacitor structure. (b) SEM cross-sectional view of 1% P(VDF-TrFE) on 10 nm SiO_2 coated with 10 nm Ti/100 nm Au. (c) Optical image of P(VDF-TrFE) showing the inconsistency of the polymer thickness, with molecular structure inset. Schematic cross-sections of the 2D NC-FET structures studied herein (d) without and (e) with an interfacial metal layer between the P(VDF- TrFE) and Al_2O_3 gate dielectric.

With the P(VDF-TrFE) integrated directly on top of the Al_2O_3 gate dielectric, there are interfacial effects that must be considered in the performance of the resulting device. As shown in Figure 21, an improvement in the SS by ~50% and a corresponding drop in the current by an order of magnitude is observed when compared to the same device operated with the substrate gate. Despite the reduction in SS through the

inclusion of the ferroelectric layer, the device operates well above the thermal limit of 60 mV/dec at 252 mV/dec, thus, not realizing the full potential of the NC-effect.

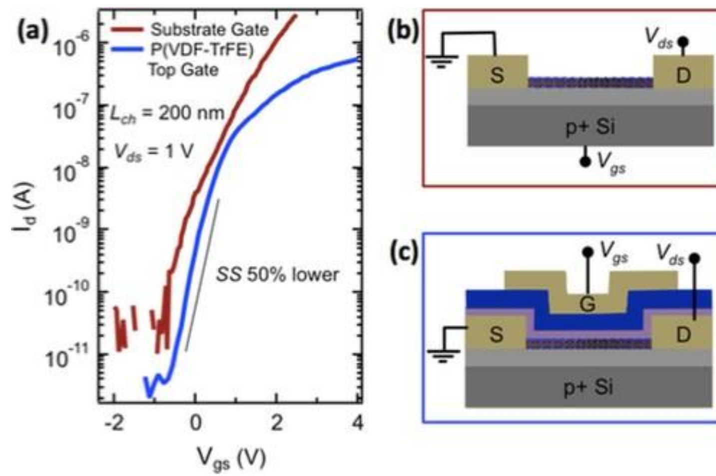

Figure 21. Performance of 2D NC-FET without interfacial metal layer. (a) Comparative subthreshold curves from the same MoS_2 channel that is gated with either the substrate as a 2D-FET or the top gate as 2D NC-FET having no interfacial layer between the P(VDF-TrFE) and Al_2O_3 dielectric. Schematics of the (b) substrate-gated and (c) top-gated configurations illustrating the characterization setup. Here, incorporating the ferroelectric polymer into the gate stack resulted in a 50% reduction in SS compared to the substrate-gated 2D FET of the same MoS_2 channel. Note that the threshold voltage of the top-gated 2D NC-FET was shifted by +4.6 V in order to provide a more useful comparison to the substrate-gated 2D FET.

However, it was previously shown that P(VDF-TrFE) is highly sensitive to interfacial effects between the polymer and the dielectric, which is most likely the cause of the poor performance.[115] Even with the reduced voltage amplification due to the interface, the ~50% reduction in the SS is still considered an effect of the ferroelectric polymer. This is because the 10 nm SiO_2 presents a more electrostatically favorable gate

as opposed to the 20 nm Al_2O_3 oxide with ~200 nm P(VDF-TrFE). This is explained by looking at the equivalent oxide thickness (EOT) of the gate stack in the 2D NC-FET.

The permittivity of the P(VDF-TrFE), ϵ_P, is strongly dependent on the polarization of the polymer, with ϵ_P reaching the thousands when fully ferroelectrically polarized. In this calculation, it is assumed that such ferroelectric polarization is not achieved – the permittivity of the polymer used is as given by the manufacturer. The EOT of the gate stack is calculated to be 79.6 nm through a comparison of the dielectric permittivities ($\epsilon_{Al_2O_3}$= 9 for Al_2O_3 and ϵ_P = 11 for P(VDF-TrFE)) and respective thickness of the materials ($t_{Al_2O_3}$for Al_2O_3 and t_P for P(VDF-TrFE)) to the permittivity and oxide thickness of SiO_2 (ϵ_{SiO_2} and 10 nm, respectively).

$$EOT = \epsilon_{SiO_2}\left(\frac{t_{Al_2O_3}}{\epsilon_{Al_2O_3}} + \frac{t_P}{\epsilon_P}\right) \qquad (24)$$

In the purely electrostatic picture, the substrate gate (EOT 10 nm) should have offered better control of the MoS_2 channel (resulting in lower SS) than the ferroelectric/dielectric top gate stack (EOT 79.6 nm).

To mitigate the deleterious effects occurring at the polymer-dielectric interface, an interfacial metal electrode was added between these layers of the gate stack. The additional electrode stops the interface from restricting with the spontaneous polarization of the P(VDF-TrFE). This permitted a more stabilized NC effect and the realization of sub-60 mV/dec switching over a wide span of drain current I_d, shown in Fig. 22. The electrode also allowed characterization of the top-

gated 2D-FET with Al_2O_3 as the gate oxide to be monitored, providing a second comparison to the baseline, substrate-gated 2D-FET and to the final 2D NC-FET.

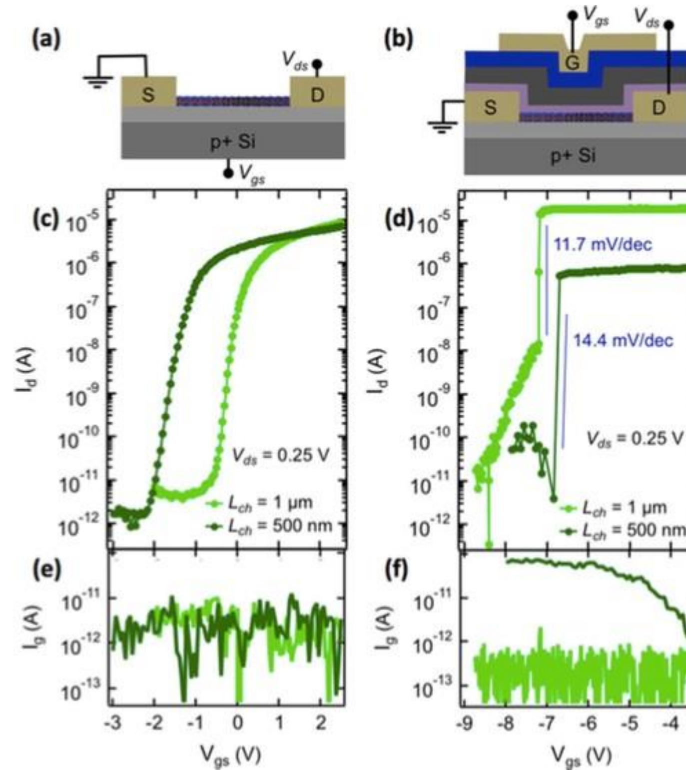

Figure 22. Performance of 2D NC-FET with interfacial metal layer. (a) Schematics of the characterization configuration for (a) substrate-gate 2D-FETs and (b) top-gate 2D NC-FETs with the interfacial metal layer. Comparative subthreshold curves from devices (c) substrate-gated and (d) top-gated show the dramatic improvement in subthreshold swing achieved with the NC gate stack. The devices in (c) and (d) use the same MoS_2 channel and contacts at the indicated channel length L_{ch}. Gate leakage current for the devices in (c) and (d) are provided in (e) and (f), respectively.

Comparison of the top-gated 2D NC-FETs with the interfacial metal layer and the substrate-gated 2D-FETs from the same MoS_2 channel afforded several key

observations. First, the substantial reduction in the SS to 11.7 mV/dec and 14.4 mV/dec in the 1 μm and 500 nm channel length devices, respectively. These improvements extend over 3–4 orders of magnitude in I_d, a result of the substantial spontaneous amplification of the applied gate voltage in modulating the surface potential of the MoS_2.

Another key observation is related to the gate leakage current I_g. Any device that exhibits a sudden and dramatic drop in I_d should ensure that it is not a result of leakage currents. In the 2D NC-FET, the leakage current remains low throughout the subthreshold region, indicating that the observed SS is not caused by gate leakage. Next, there is a negative shift in threshold voltage for both of the 2D NC-FETs when compared to their substrate-gated counterparts. A large number of factors could influence this shift, most impactful of which is the presence of charge traps and fixed charge introduced by the ALD-grown Al_2O_3 gate dielectric. Evidence of this being the primary cause of the threshold voltage shift is found in the comparison of the subthreshold curves for a device operated with the substrate gate, interfacial metal gate, and top gate, wherein operation with the interfacial metal gate (top-gate with Al_2O_3 but no ferroelectric) already results in a negative threshold voltage shift of approximately 12 V, as shown in Fig. 23. Finally, Fig. 22 shows that there is an inconsistent change in the on-current for the 2D NC-FETs compared to their substrate-gated operation. The 1 μm

device has a slight increase in drain current, while the 500 nm device exhibits a decrease of approximately an order of magnitude.

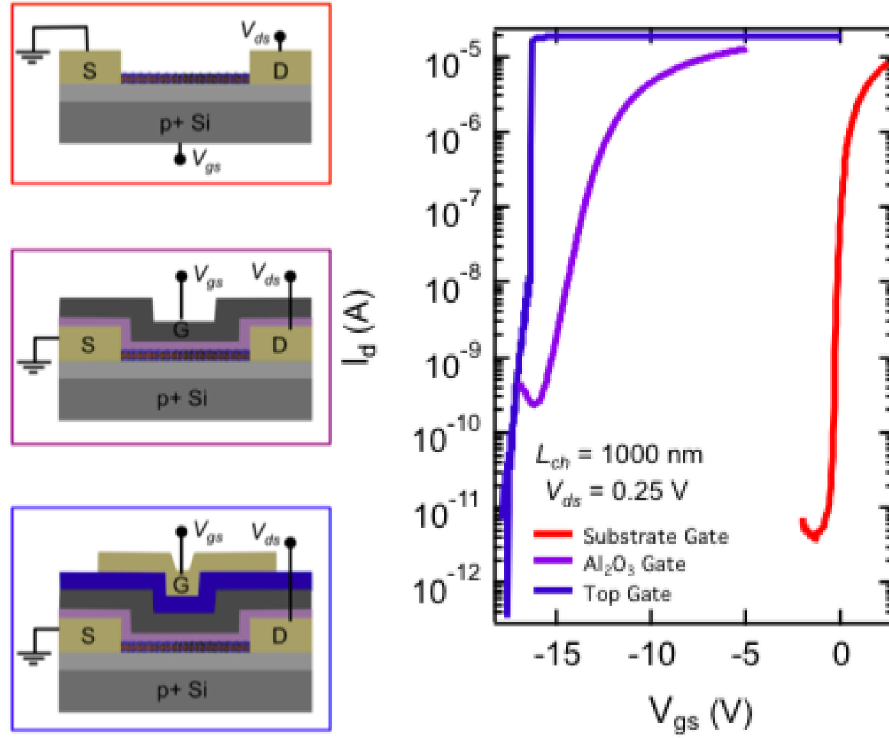

Figure 23. Comparison of performance for the same MoS_2 channel under three different gating configurations. The 2D NC-FET gating configurations are schematically shown on the left: substrate gate (red), interfacial metal gate with only Al_2O_3 dielectric (purple), and top gate with full NC gate stack (blue).

Unfortunately, further characterization of the 2D NC-FETs was hindered by degradation of the P(VDF-TrFE). Immediately following the initial sweep, the performance of the 2D NC-FET degraded, no longer exhibiting sub-60 mV/dec switching and rendering it impossible to extract useful information regarding hysteresis, etc. The

immediate degradation of the 2D NC-FET is shown in Fig. 24, where the performance of the initial 2D NC-FET is compared to the substrate gated 2D-FET and to the degraded 2D NC-FET.

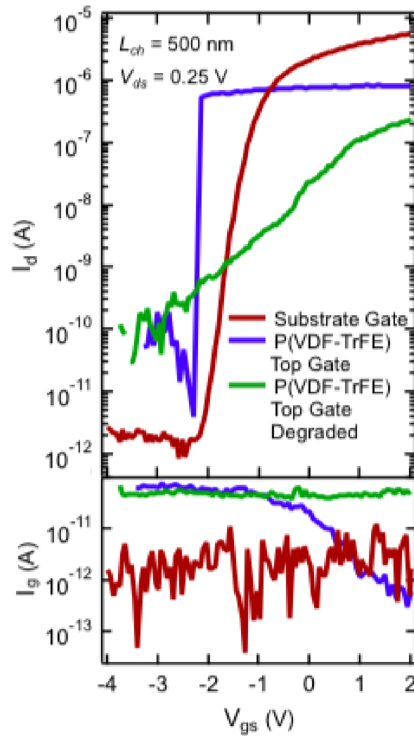

Figure 24. Subthreshold curves showing the immediate degradation of the 2D NC-FET after the initial sweep (note that the blue and green curves have been shifted by +8 V for better comparison). The substrate gate curve is the baseline device. The blue curve is the first full sweep from positive to negative gate voltage of the 2D NC-FET (with interfacial metal layer). The green curve represents a subsequent sweep of the 2D NC-FET showing marked degradation compared to the initial curve that is attributed to instability of the ferroelectric polymer.

The sub-60 mV/dec switching cannot be attributed to the degradation of the P(VDF-TrFE) as there is the interfacial metal layer and the 20 nm Al_2O_3 are components of the gate stack separating the polymeric ferroelectric from the channel. Further, the gate leakage current remains steady over the range of operation for all characterization sweeps of the 2D NC- FETs.

The considerable improvement in SS for these 2D NC-FETs is promising but unstable. All devices that exhibited steep switching behavior immediately degraded upon further characterization. Such breakdown is not unique for the polymeric ferroelectric. Unfortunately, this made it impossible to study the hysteresis behavior in these 2D NC-FETs, as the return sweep of the reported curves already displayed the degraded behavior. While the interfacial electrode between the ferroelectric and dielectric in the gate stack has been shown to improve ferroelectric behavior, these devices do not allow for such postulation to be validated. Aside from rendering it impossible to obtain more detailed characterization data from the devices, this breakdown of the ferroelectric behavior in the P(VDF-TrFE) is obvious evidence of unreliability for use in a FET technology. Though it provided initial results of sub-60 mV/dec switching in 2D NC-FETs, future work should make use of the more technologically relevant and reliable doped-HfO_2 ferroelectrics.

5.4 Conclusion

Replacing the 3D silicon channel of an NC-FET with 2D TMD MoS_2 enabled subthreshold swings well below the thermal limit (down to 11.7 mV/dec) that extend over several orders of magnitude in drain current. The inclusion of the electrode between the polymeric ferroelectric and gate dielectric proved to be crucial when realizing sub-60 mV/dec switching. The ferroelectric was integrated into the gate stack rather than a separate capacitor electrically added. The polymeric 2D NC-FET demonstrated superb low voltage switching behavior; however, the P(VDF-TrFE) ferroelectric polymer proved to be unstable beyond initial testing. Overall, this was the first experimentally demonstrated 2D NC-FET and set the stage for further exploration.

6. 2D NC-FET using TiN/HZO/TiN

6.1 Introduction

Some of the most encouraging recent progress in Si-based NC-FETs has been a result of the CMOS-compatible HZO ferroelectric.[20,102] Doped hafnium oxide thin films are simple, binary oxides with a non-perovskite crystal structure and relatively low permittivities that can be grown using CMOS-compatible atomic layer deposition (ALD) processes. Zr-doped HfO_2 films are favored for integration into CMOS technology for chemical and physical similarities to HfO_2 and low crystallization temperatures. With top and bottom titanium nitride (TiN) electrodes, Zr-doped HfO_2 films have been found to exhibit the largest remnant polarizations when in a 1:1 Hf:Zr ratio, $HfZrO_2$ or HZO, in films thinner than 10 nm.[20,71] HZO exhibits an inverse scaling behavior of polarization versus thickness compared to other prominent ferroelectrics; for HZO, polarization is enhanced as the thickness is scaled.

While the previous chapter demonstrated the first experimental integration of a ferroelectric in the gate stack of a 2D MoS_2 FET to create a 2D NC-FET yielding sub-60 mV/dec switching[116], the demonstrated device used an unstable polymeric ferroelectric that led to rapid degradation of the device and the inability to fully characterize its behavior, including such critical aspects as hysteresis. Replacing the ferroelectric polymer with a more technologically relevant, reliable ferroelectric, like HZO, is needed to study the true performance and operation of the 2D NC-FET. This chapter presents

experimental data from bottom-gated 2D NC-FETs that use a TiN- HZO-TiN MFM in the gate stack. The result is a reproducible sub-60 mV/dec switching behavior and stable devices that allowed for detailed characterization.

6.2 Experimental Details

Titanium nitride was grown using a custom-built Kurt J. Lesker plasma-enhanced ALD (PE-ALD) cluster system using precursors tetrakis(dimethylamino)titanium (IV) ($Ti[N(CH_3)]_4$) (TDMAT) and a nitrogen (N_2)/hydrogen (H_2) plasma on an undoped silicon wafer. The ALD chamber was heated to 214°C and the TDMAT precursor to 79°C. The TDMAT had pulse/Ar purge times of 0.5 s/10 s, respectively. The wafer was then exposed to the plasma for 30 s, followed by a 20 s Ar purge. This was continued for 135 cycles to grow 10 nm TiN. Immediately following deposition, the ALD chamber was heated to 271°C for hafnium zirconium oxide ($HfZrO_2$, or HZO) growth. The hafnium precursor tetrakis(dimethylamino)hafnium ($Hf(N(CH_3)_2)_4$) (TDMAH) was heated to 85°C and the zirconium precursor tetrakis(dimethylamino)zirconium(IV) ($Zr(N(CH_3)_2)_4$) (TDMAZ) to 75°C. Water vapor was used to form the oxides. HZO films were grown in a 1:1 Hf:Zr ratio by alternating cycles of TDMAH, water vapor, TDMAZ, water vapor with pulse/purge times of 20 ms/10 s, 140 ms/10 s, 200 ms/20 s, and 140 ms/10 s, respectively. The alternating cycles were repeated 66 times for ~12 nm HZO growth or 100 times for ~15 nm HZO growth. After completion, the ALD chamber was cooled to 214°C, and the

TiN growth was repeated to form the base TiN/HZO/TiN MFM capacitor of the 2D NC-FET.

Photoresist S1805 was spin-coated on the MFM capacitor at 500 rpm for 5 s, 4000 rpm for 60 s and baked at 115°C for 60 s. Photolithography was employed to create the capacitor patterns. After a 5.5 s exposure, the wafer was developed in MF:319 for 10 s. The top TiN layer was etched from the area surrounding the pattern with a reactive ion etch (RIE) of 36 sccm BCl_3 and 84 sccm Ar with 100 W inductively coupled plasma (ICP) power and 500 W RIE power for 18 s in a 70 mTorr atmosphere. The HZO was removed from the non-patterned area with a 90 s buffered oxide etch (BOE), exposing the bottom TiN layer for characterization. The remaining resist was removed in a beaker of acetone heated to 80°C for ~4 hours. Initial P-E characterization was completed with a Radiant Technologies, Inc. RT66B Ferroic Tester to confirm the linear behavior of the HZO. Capacitors that displayed linear behavior were subject to a rapid thermal anneal (RTA) between 550-600°C for 30 s. P-E characterization with the Ferroic Tester was repeated to confirm ferroelectricity via the hysteretic behavior of the curve. A schematic of the PE-ALD chamber and the MFM capacitors, along with P-E characteristics for different annealing temperatures are given in Fig. 25.

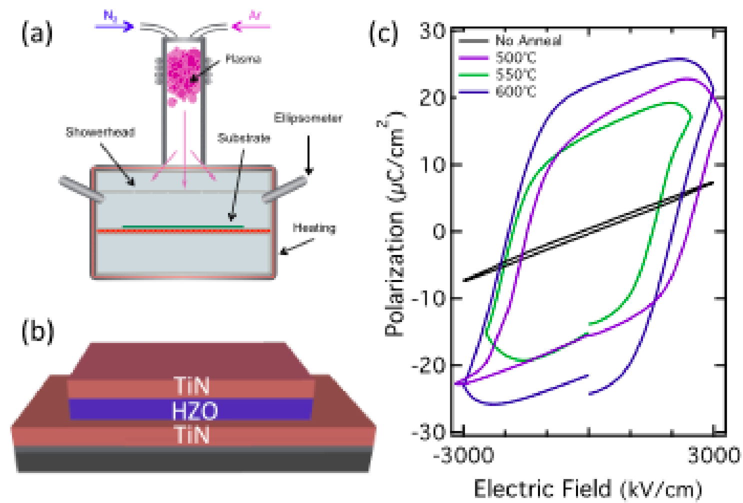

Figure 25. TiN-HZO-TiN capacitor schematics and ferroelectric behavior. Schematics of (a) PE-ALD system showing N_2 plasma and Ar carrier gasses and (b) TiN-HZO-TiN capacitor, and (c) P-E characteristics of the MFM capacitors before and after annealing at different temperatures.

After MFM testing, the ALD chamber was set to 225°C and approximately 10-27 nm HfO_2 was deposited on the capacitors. The HfO_2 was thermally grown from TDMAH and water vapor with pulse/purge times of 200 ms/10 s and 140 ms/10 s, respectively for 115 cycles (~10 nm), 225 cycles (~20 nm), or 300 cycles (~27 nm). PMMA 950 A3 was spin- coated over the HfO_2 at 500 rpm for 5 s and 4000 rpm for 60 s, then baked at 180°C for 180 s. The alignment mark pattern was written using electron beam lithography (EBL) in a 600 μm field of view with 60,000 exposure points. The electron beam was set to a 2 nA current with an exposure of 0.45 μs to create a dose of ~1145

μC/cm^2. The pattern was developed in a 3:1 ratio of IPA to MiBK for 120 s, rinsed with IPA, and dried with nitrogen gas. The alignment pattern was metallized employing an electron beam evaporator with 5 nm Ti, 30 nm Au. Lift-off was performed in a beaker of acetone heated to 80°C for ~5 minutes. The wafer was rinsed with IPA and dried under nitrogen gas.

MoS_2 was mechanically exfoliated over the patterned regions. MoS_2 flake thicknesses were optically characterized and confirmed with AFM, with flake thicknesses nominally chosen between ~5-9 nm for device fabrication. PMMA 950 A3 was spin-coated over the capacitors with MoS_2 at 500 rpm for 5 s and at 4000 rpm for 60 s, then baked at 180°C for 60 s. The same PMMA/EBL/development process previously described was employed to write the contacts and leads in the same step. Once written and developed, the contacts and leads were metallized with 25 nm Ni. Lift-off was performed in a beaker of acetone heated to 80°C for ~15 minutes. The wafer was rinsed with IPA and dried under nitrogen gas. The PMMA/EBL/development process was again repeated to create the S/D pads, followed by metallization using an electron beam evaporator with 2 nm Ti/15 nm Pd/20 nm Au. Lift-off was performed in a beaker of acetone heated to 80°C for ~5 minutes. The 2D NC-FETs and the MoS_2 2D-FETs were characterized with an Agilent (Keysight Technologies) B1500A Semiconductor Parameter Analyzer.

6.3 Results and Discussion

In order to realize ferroelectricity in HZO films, TiN interfacial layers were employed with an annealing step to drive formation of the orthorhombic crystal phase. The TiN metallic electrodes sandwiched the HZO, where the topmost TiN layer (the interface between the HZO and HfO_2) served as an internal gate electrode (V_{int}). The V_{int} electrode was previously shown to be crucial for mitigating interfacial effects that arise between the ferroelectric and gate oxide. The inclusion of this layer in device structures also allowed for characterization of the same MoS_2 channel as a traditional, bottom-gated 2D-FET for comparison to a 2D NC-FET. Additionally, the V_{int} layer allowed for monitoring of the internal voltage gain (change in V_{int} versus change in applied V_{gs}) during operation of the 2D NC-FET. The general layout of the devices is given in the scanning electron microscopy (SEM) image in Fig. 26(c), where multiple L_{ch} were included on the same MoS_2 flake.

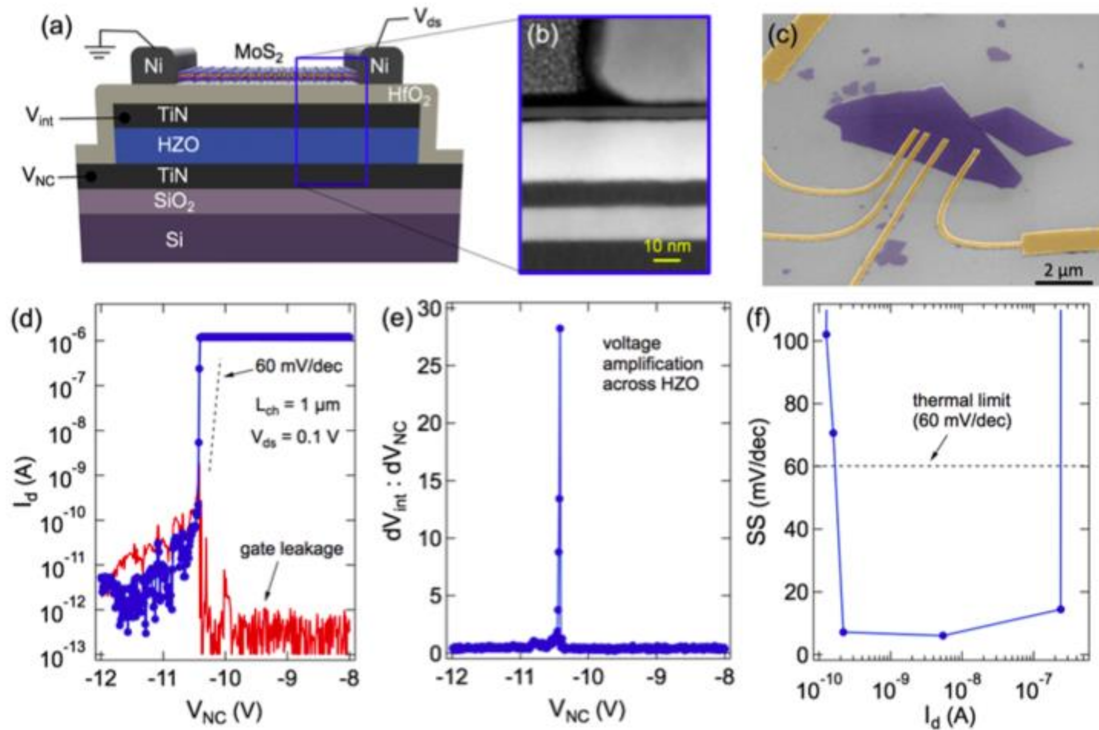

Figure 26. 2D negative capacitance FET with sub-60 mV/dec switching. (a) 2D NC-FET device schematic illustrating characterization configuration. (b) STEM image showing the layers and thicknesses of the gate stack, the individual MoS_2 layers, and a portion of the Ni electrode. (c) False- colored, tilted SEM image of MoS_2 channel and contacts (20 nm Ni) over MFM-oxide gate stack. (d) Subthreshold curve of 2D NC-FET plotted with gate leakage current. (e) Dramatic increase in V_{int} with respect to the applied V_{NC} occurring in the region of sub-60 mV/dec switching as is characteristic of the NC effect. (f) Point-by-point subthreshold swing (SS) vs drain current showing the sub-60 mV/dec switching extending over more than four decades.

The subthreshold characteristics of a 2D NC-FET with an MoS_2 thickness of ~5 nm (having 10 nm HZO, 10 nm HfO_2, 1 μm channel length (L_{ch}), and drain-source bias (V_{ds}) of 0.1 V) are given in Fig. 26(d-f). In this configuration, V_{NC} is the gate, V_S is the grounded source, and V_{int} is a floating gate that allowed the voltage at the V_{int}

electrode to be measured while characterizing the 2D NC-FET. The SS remains below the 60 mV/dec limit for over 4 decades of current, with a minimum of 6.07 mV/dec and an average of 8.03 mV/dec. Along with the drop in I_d at V_t, there is a simultaneous increase in the leakage current (I_g) that is attributed to the amplified gate field across the oxide. This amplification is seen through the change in the voltage on V_{int} with respect to the change in applied gate voltage (V_{NC}), which increases ~28x in the region of sub-60 mV/dec switching, as shown in Fig. 26(e). The gain observed at V_{int} with the 2D NC-FET is a significant increase over that observed from 3D NC-FETs, which generally demonstrate a maximum improvement of less than 7x.[2,5,6] The large amplification is partially attributed to the more stable C_s from the 2D MoS_2.

The abrupt and dramatic switching behavior displayed in Fig. 26(d) is a direct effect of integrating a ferroelectric layer into the gate stack, previously shown to stem from the small region in the simulated P-E curve of the ferroelectric material where the ferroelectric voltage is of opposite polarity to the applied voltage for a given I_d. Mathematically, these changes are explained through the Landau-Khalatnikov (L-K) equation, which relates the polarization to the applied field, the voltage across the ferroelectric (V_{Fe}), and the ferroelectric thickness (t_{Fe}):

$$E = 2aP + 4bP^3 + 6cP^5 = \frac{V_{Fe}}{t_{Fe}} \qquad (25)$$

The *a* parameter is material- and temperature-dependent, while *b* and *c* are strictly material-dependent parameters. For ferroelectric operation, *a* has a negative value, while *b* can be either positive or negative. *c* is considered to be always positive. Simulations using the L−K equation show a brief region where the voltage across the ferroelectric is of opposite polarity to that of the applied voltage, indicating the negative capacitance effect that produces steep switching (shown in Figure 27).[2,6]

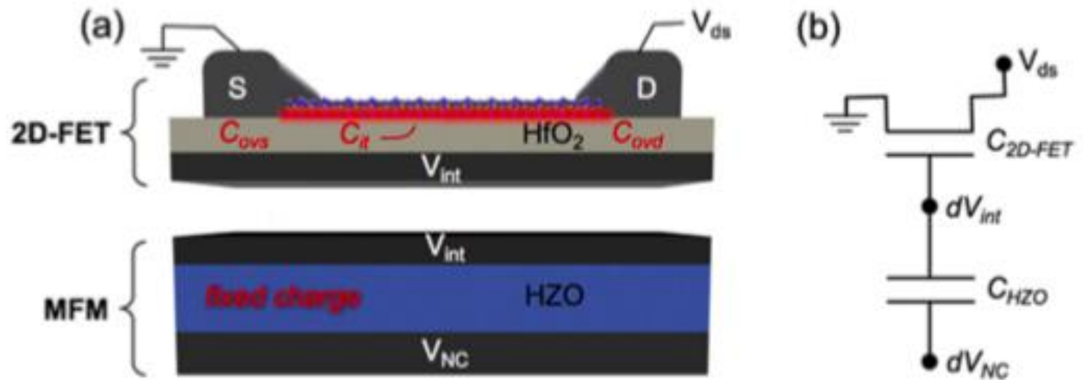

Figure 27. Voltage and capacitor network in 2D NC-FET. (a) Device schematic split into the metal–ferroelectric–metal (MFM) capacitor and the 2D-FET. Indicated in red are some of the sources of parasitic behavior in the device, including overlap capacitance between the source/drain and V_{int} (C_{ovs} and C_{ovd}), fixed charges, and interface traps (with associated C_{it}). (b) Diagram of the 2D NC-FET gate stack showing the primary voltages and capacitances. Note that the $C_{2D\text{-}FET}$ includes the capacitance from the HfO_2 gate dielectric as well as the capacitance from the MoS_2 channel (C_s).

This also explains the observed voltage amplification behavior. With the ferroelectric in series with the 2D-FET, the change in the applied voltage (dV_{NC}) can be

written as the sum of the differential voltages between the ferroelectric material (dV_{Fe}) and the 2D-FET (dV_{int}):

$$dV_{NC} = dV_{Fe} + dV_{int} \quad (26)$$

Thus, a change in dV_{Fe} opposite in polarity to that of the applied V_{NC} causes the differential potential felt at the 2D channel (dV_{int}) to be larger than V_{NC}.

Further characterization of the 2D NC-FET revealed some interesting dependencies on V_{ds}, as seen in Fig. 28. All V_{ds} conditions achieved sub-60 mV/dec switching; however, the larger applied V_{ds} produced a lower minimum SS and a larger range over which steep switching occurred. A similar observation was made for the hysteresis; as V_{ds} increased, hysteresis decreased until negligible. The effect of V_{ds} on hysteresis can be explained as a drain-side switching phenomenon, where a reduction in V_{NC} causes the gate-to-drain voltage (V_{gd}) to rise. The overlap in the device structure (source and drain contacts are overlapping the gate stack as shown in Fig. 26(a)) prompts the largest field to drop at the drain. At some V_{gd}, the ferroelectric switching depletes the region under the drain, creating an abrupt decrease in I_d. With larger V_{ds}, the depletion occurs much closer to V_t, lowering the hysteresis. This drain-side switching effect can be mitigated by employing a self-aligned gate, which minimizes the overlap between the gate and drain to reduce the impact of the drain on channel switching.

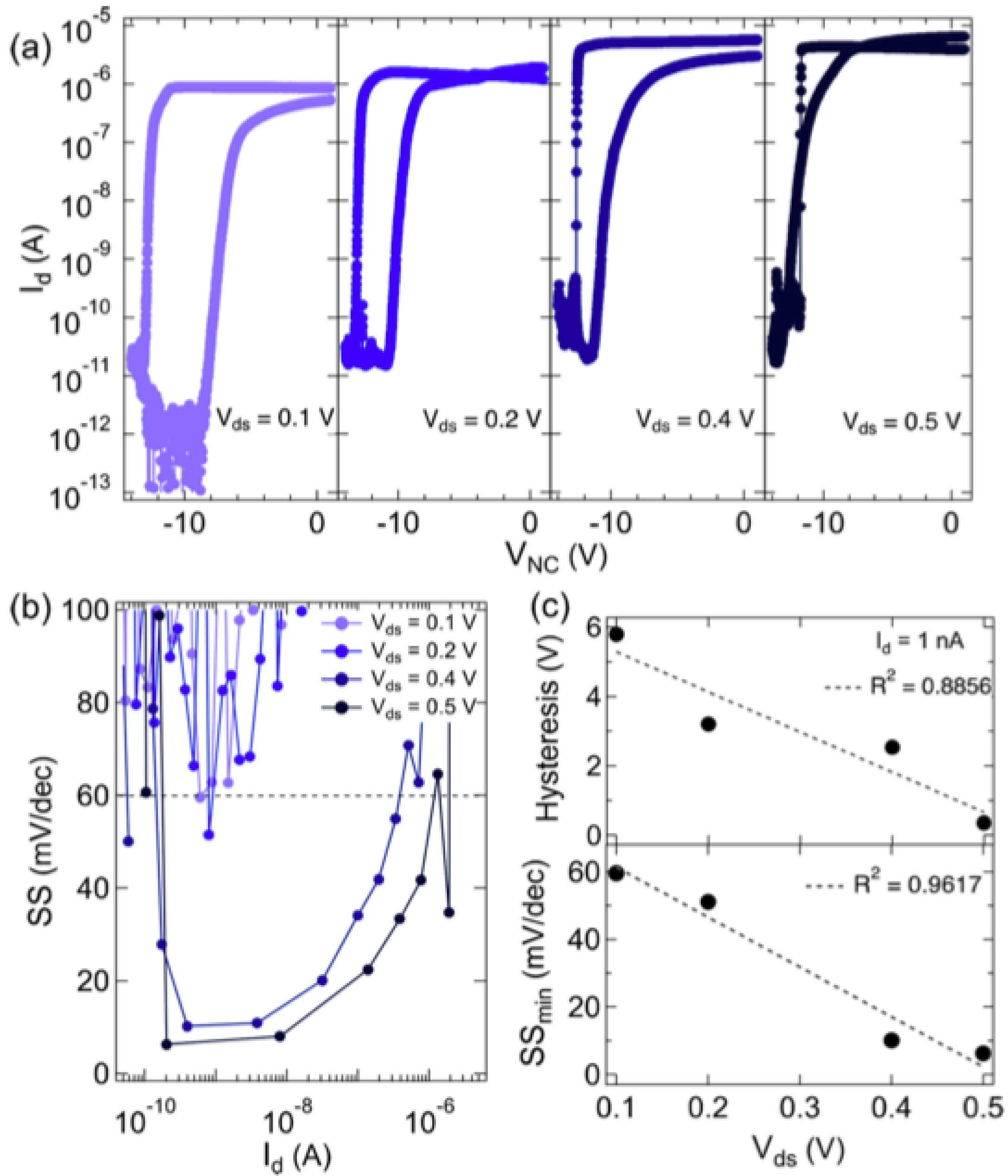

Figure 28. Drain bias-dependent behaviors of hysteresis and SS in 2D NC-FETs. (a) Hysteretic subthreshold curves of a 2D NC-FET at increasing V_{ds} (L_{ch} = 1 μm). (b) Point-by-point subthreshold swing vs drain current showing decreasing SS with increasing V_{ds}. (c) Top: decrease in hysteresis with increasing V_{ds}. The hysteresis was measured at $I_d = 10^{-9}$ A. Bottom: minimum SS dependence on V_{ds}.

An additional aspect of the hysteretic behavior in these devices is that the sub-60 mV/dec switching occurs exclusively on the negative sweep, whereas the positive sweep exhibits a more traditional subthreshold response. This asymmetry in the curves based on sweep direction results from the presence of charge traps in the gate stack heterostructure, which minimize polarization effects by screening the electric field. After the traps have been neutralized, the ferroelectric becomes polarized, resulting in the abrupt jump that is able to be observed in the reverse sweep. However, for the positive sweep, any such rapid polarization is stifled by the emptying/charging of traps that leads to a more gradual switching behavior.

The subthreshold performance of a MoS_2 2D-FET with ~8 nm MoS_2 is compared to that of the respective 2D NC-FET (on the same MoS_2 channel) in Fig. 29. The characterization of the 2D-FET was accomplished by using V_{int} as the gate electrode. Comparison of the same 500 nm channel transistor at V_{ds} = 1 V demonstrates the advantageous switching behavior of the 2D NC-FET. A dramatic improvement of almost two orders of magnitude is seen in the SS of the 2D NC-FET (minimum SS = 8.5 mV/decade) when compared to that of the 2D-FET (minimum SS = 161 mV/decade). Direct comparison of these devices shows improvement in subthreshold characteristics from the NC-effect and indicates that detrimental interfacial effects were minimized. In all, Fig. 29 suggests improvement in subthreshold characteristics is strictly due to the addition of the ferroelectric layer and the realization of the NC-effect.

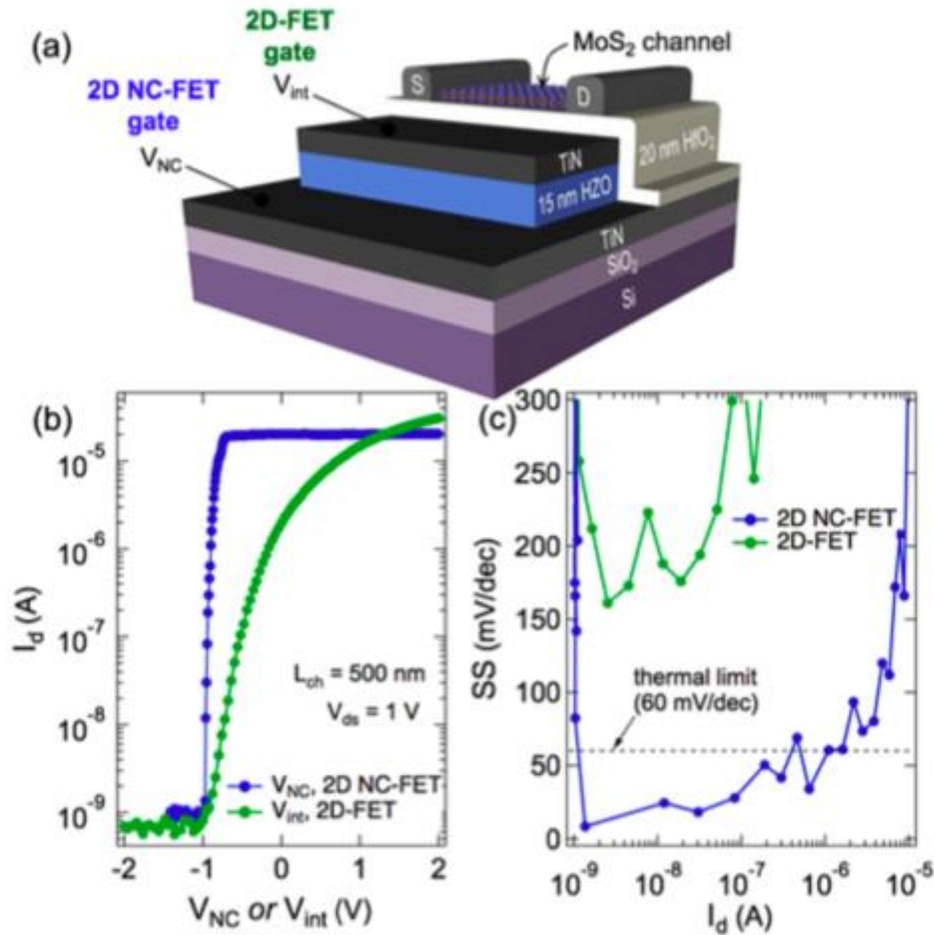

Figure 29. Comparison of 2D NC-FET with 2D-FET on same MoS_2 channel. (a) Cross-sectional schematic of the device illustrating V_{int} and V_{NC} terminals. (b) Subthreshold curves from the same MoS_2 channel gated either as a 2D-FET (using V_{int} as the active gate) or as a 2D NC-FET (using V_{NC}). Note the threshold voltage of the 2D NC- FET was shifted positive to match up with that of the 2D-FET for a more useful comparison. (c) Subthreshold swing from the 2D-FET and 2D NC-FET. The 2D-FET operates well above the thermal limit, while the 2D NC-FET has a large range in drain current where the SS is below 60 mV/dec

The HZO thickness of the device in Figure 29 was increased from 12.3 to 18.6 nm to avoid any unfavorable effects from non-uniform HZO deposition across the wafer. The HfO_2 thickness was also increased from ~22.8 to ~45.7 nm, to ensure complete coverage of the MFM stack. Note that these film thicknesses were verified by extraction from cross-sectional scanning tunneling electron microscopy (STEM) images, such as the one shown in Figure 26(b). Energy dispersive spectroscopy (EDS) analyses of the device structure was collected (Figure 30) while obtaining STEM images. The EDS yielded a detailed elemental map to show the distinction between layers and provide evidence for no perceivable diffusion between the critical layers of the gate stack (note, oxygen and nitrogen appear more throughout the spectra because of the presence of these molecules in ambient conditions).

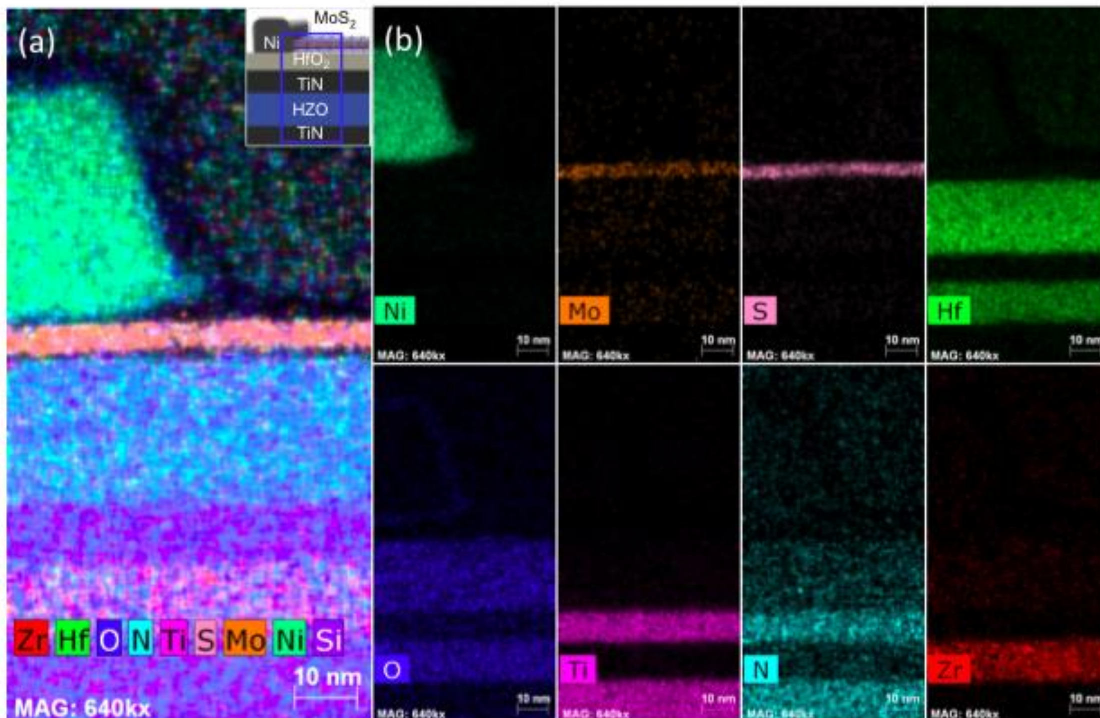

Figure 30. EDS analysis of the elements present in each layer of the 2D NC-FET. (a) Composite EDS image of the gate stack with Ni contact electrode. The apparent presence of silicon in some regions is because the silicon peak in the EDS spectrum is close to the hafnium peak. (Inset) Schematic of device area where EDS was taken. (b) EDS analysis mapping the locations of each element within the device structure. All elements are mostly confined to their individual layers, except oxygen and nitrogen. The increased proportion of these elements is due to their presence in ambient conditions.

Also, note that the subthreshold curve of the 2D NC-FET in Figure 29(a) has been shifted by ~26 V to provide a more useful comparison between the 2D NC-FET and 2D-FET that are using the same MoS_2 channel.

The large negative shift in threshold voltage for the 2D NC- FET compared to the 2D-FET stems from a combination of factors, including the capacitance from the overlapping source/drain contacts with the gate (illustrated in Figure 27) and trapped charges in the HZO and HfO_2 layers. To determine the impact of the overlap capacitance on the threshold voltage shift, a model was developed for the 2D NC-FET using industry standard BSIM-IMG compact model for the base MoS_2 device coupled with the L-K equation to describe the behavior of the ferroelectric. The results of the model are shown in Figure 31.

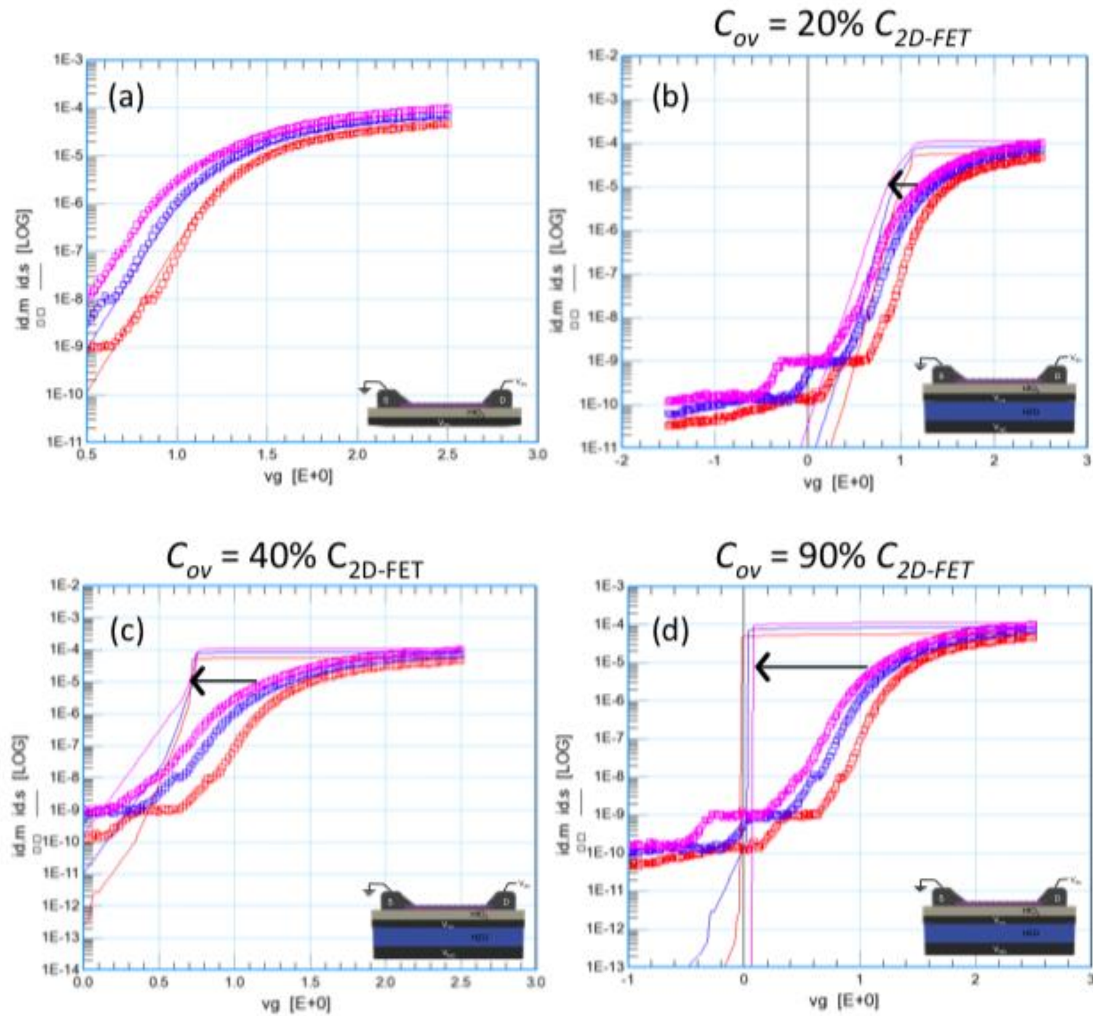

Figure 31. 2D NC-FET simulation exploring the effects of overlap capacitances. (a) 2D-FET simulation (solid line) fit to match experimental data (circles). (b) Simulated 2D NC-FET (solid line) with the overlap capacitance at 20% of the 2D-FET capacitance, plotted with the experimental 2D-FET data and showing slight threshold voltage shift. (c) Overlap capacitance increased to 40% with more negatively shifted threshold voltage. (d) Overlap capacitance increased to 90% with significant reduction in SS and large threshold voltage shift. All insets show schematics of simulated device.

The results of the model give evidence that an increase in the overlap capacitance (C_{ov}) results in a more negative threshold voltage shift. There was a limitation on the amount of C_{ov} that could be introduced in the model, and a C_{ov} between 20% to 90% of the 2D-FET capacitance ($C_{2D\text{-}FET}$) was investigated. The actual C_{ov} in the fabricated 2D NC-FETs was even larger than 90% of $C_{2D\text{-}FET}$ since the entire source and drain contact pads overlap with V_{int}. However, C_{ov} is still not solely responsible for the observed negative shift in threshold voltage, as the presence of trapped charges within the HZO and/or the HfO_2 layers was also identified as a contributing factor. This was confirmed by comparing 2D NC-FETs fabricated with different thicknesses of the HZO and HfO_2 (both layers were scaled concurrently). When the HZO was increased in thickness by ~50% and HfO_2 by ~100%, the negative shift in threshold voltage more than doubled. Since the relative C_{ov} compared to $C_{2D\text{-}FET}$ would be nominally consistent for these devices, this result gives evidence for the substantial impact that the HZO and HfO_2 thicknesses play in the observed threshold shift. As thinning the HZO will bring V_t closer to 0 V, the recent demonstrations of sub-2 nm HZO exhibiting ferroelectricity is very encouraging for future iterations of these devices.[20]

Additional fabricated devices point to the reliability and repeatability of the NC effect in 2D NC-FETs. The subthreshold characteristics of 2D NC-FETs using another MoS_2 flake ~7 nm thick are given in Figure 32.

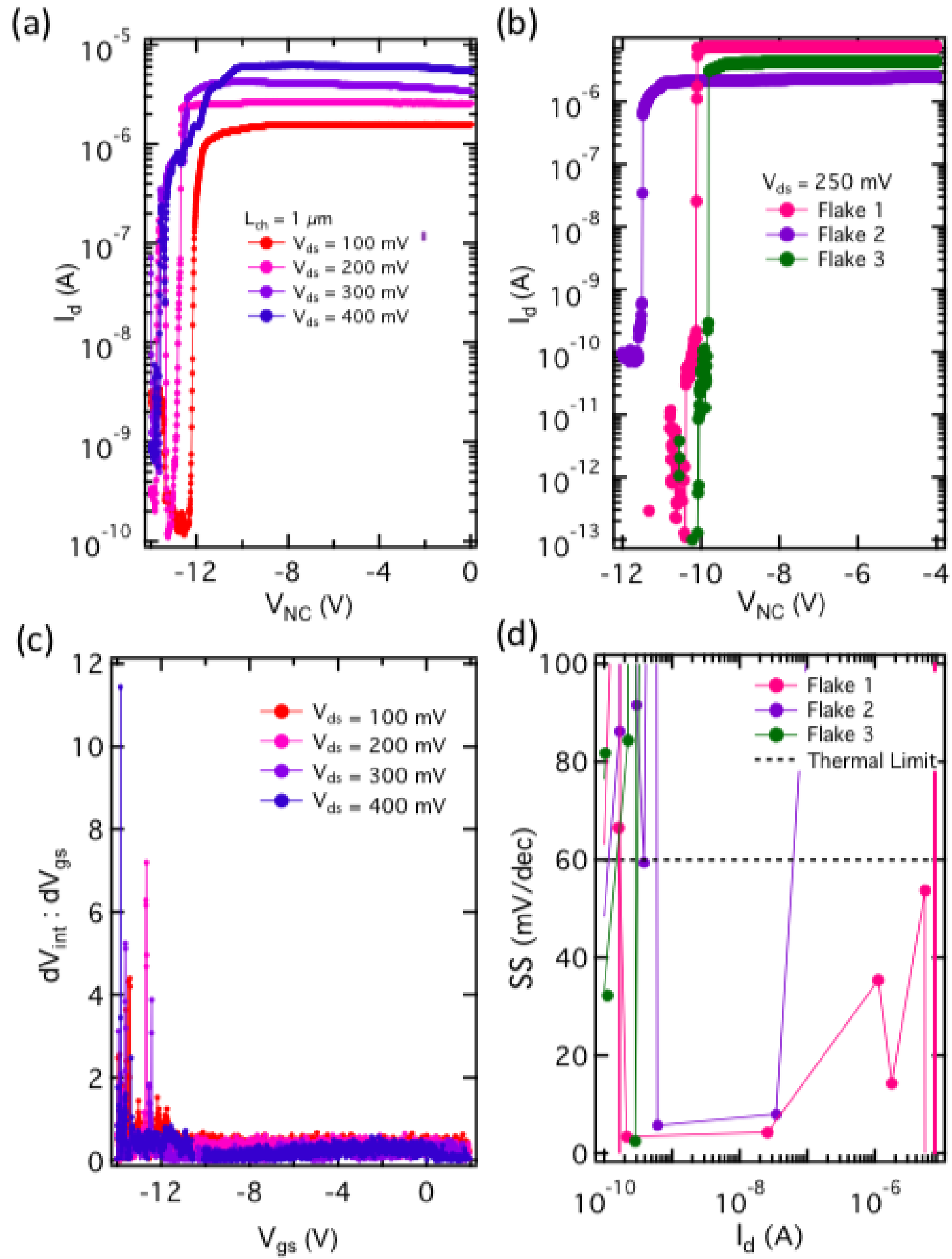

Figure 32. Characterization of additional 2D NC-FETs. Subthreshold curves (a) from the same channel at different V_{ds} and (b) from 200 nm (pink), 500 nm (purple), and 1 μm (blue) L_{ch} across different MoS_2 flakes, (c) increases in the change in V_{int} with respect to V_{NC} for each V_{ds} in (a), and (d) point-by-point subthreshold swing per drain current showing all devices operate well below the thermal limit.

Here, the ferroelectric and HfO_2 thicknesses were 12.3 and 22.8 nm, respectively, and L_{ch} = 500 nm. Providing for variations across different MoS_2 flakes, this device displays comparative performance to that shown in Figure 27(a), where a sub-60 mV/dec SS is achieved at each V_{ds}. The observed voltage gains (dV_{int}/dV_{NC}) again occur at V_t, as seen in Figure 32(c). Decreases observed in the gain compared to the device in Figure 26(e) are attributed to current leakage along the grain boundaries of the thicker ferroelectric in the MFM capacitor. This type of leakage produces "leaky" ferroelectric behavior, where the edges of the P−E characteristics are slightly rounded, as shown from the 600 °C anneal characteristic in Figure 27(c). Regardless of the drop, the voltage gain at each V_{ds} is still comparable to, if not greater than, that of reported NC-FETs from 3D silicon channels.[5,61,63,64,108]

The effects of varying the sweep rate on the subthreshold characteristics were also investigated. These devices utilized the thicker HZO and HfO_2 films of 18.6 and 45.7 nm, respectively. Hysteresis curves at measurement lengths of 6, 8, and 10 μs corresponding to sweep rates of 19.84, 16.88, and 11.90 Hz, respectively, are provided in Figure 33. The data was obtained from the same 2D NC-FET, with all other device parameters held constant. Of most importance are the linear shifts observed in the threshold voltages and in the hysteresis in Figure 33(b). Shorter measurement times (higher sweep rates) lowered the hysteresis present in the device, yet had no effect on either I_{OFF} or on the return sweep V_t. While this effect requires further investigation to

interpret its precise/quantitative origin, it is attributed to interface traps in the gate stack, especially since the sweep rate dependence of hysteresis in a traditional MFM is typically opposite the observation in these devices (hysteresis for MFMs increases with sweep rate). In this case, the small changes in sweep rate explored in Figure 33 are modulating the impact of interface traps based on the trap charging rates–a longer voltage pulse duration (slower sweep rate) allows for more traps to charge and thus yields more hysteresis.

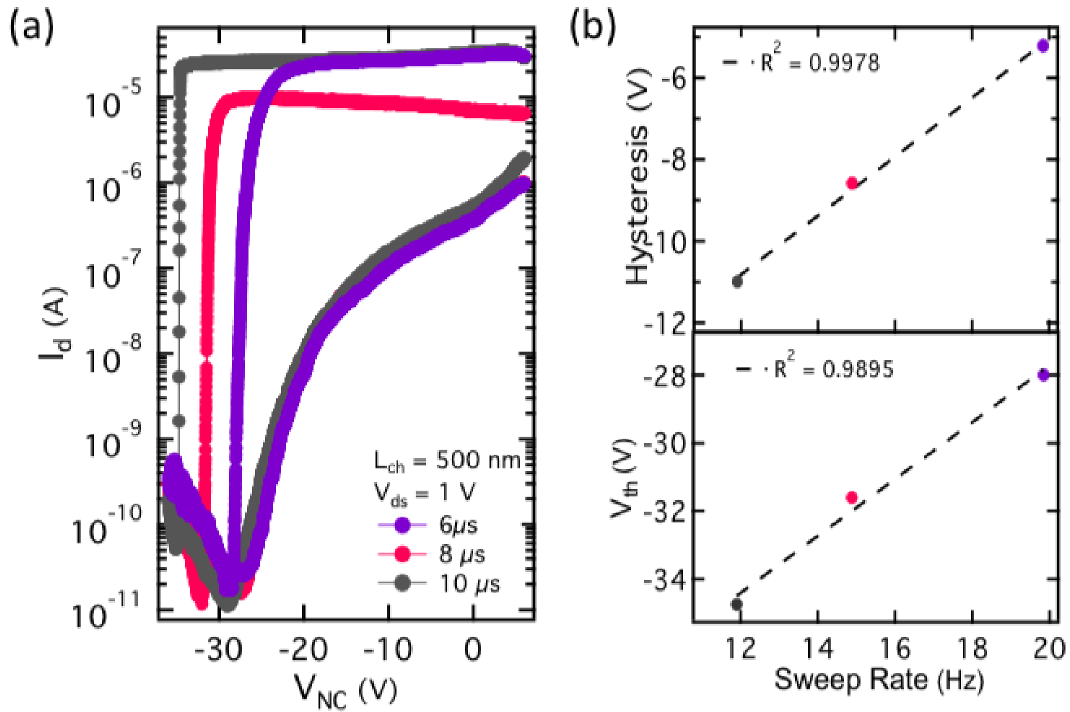

Figure 33. Sweep rate dependence of 2D NC-FET subthreshold characteristics. (a) Subthreshold curves from the same device with different sweep rates. 6, 8, and 10 μs

correspond to the length of time per data point. (b) Top: decreasing hysteresis with increasing sweep rate (faster sweeps). Bottom: decreasing threshold voltage with increasing sweep rate.

This has been observed in other nanomaterial-based FETs, where small decreases in the sweep rate yielded significant increases in hysteresis.[117] As nanomaterials offer no surface bonding to their supportive oxide substrate, they tend to be more prone to deleterious interface trap effects such as these. A more optimal 2D NC-FET device will be one that has minimized the interface trap density so as to minimize its impact on operation in these ways.

6.4 Conclusion

In conclusion, 2D NC-FETs with repeatable, sustained sub-60 mV/dec switching have been demonstrated using 2D MoS_2 channels and CMOS-compatible HZO ferroelectric. The 2D MoS_2 provides the most scalable channel to stabilize the NC-effect and achieve large voltage gains, resulting in SS below the thermal limit over more than four orders of magnitude of drain current. Extensive improvement in subthreshold performance was shown with the 2D NC-FET compared to a 2D-FET on the same MoS_2 channel. Shifts in V_t were found to be directly correlated to HZO thickness—the thinner the HZO the lower (closer to 0 V) the V_t. Analysis of hysteresis, including its dependence on bias and sweep rate, and of the voltage gain were also included. These results show the great promise that 2D NC-FETs have for scalable, low-voltage transistors using a CMOS compatible ferroelectric layer.

7. 2D NC-FET Without TiN Interfacial Layers

7.1 Introduction

Over the past few years, there has been a surge of research into NC-FETs that utilize doped hafnium oxide thin films as the ferroelectric, resulting from the numerous benefits of this material, with emphasis on CMOS compatibility and the increased ferroelectric response at scaled thicknesses.[20,71,111,118,119] Many devices employing HZO have included a metallic interfacial layer into the design to mitigate any adverse interfacial effects and hinder the emergence of a passive layer that suppresses ferroelectricity.[20,68,118,120] Recently, it was discovered that the metallic layer introduces an overlap capacitance that affects device performance, leading some researchers to investigate NC-FETs without an interfacial layer.[118,121]

There have now been NC-FETs with the HZO in direct contact with the dielectric oxide showing small regions of sub-60 mV/dec switching.[119] In fact, since the publication of the first 2D NC-FET (see Chapter 5),[116] several other groups have reported 2D NC-FETs without the interfacial metal layer and, correspondingly, without an extensive sub-60 mV/dec switching region.[19,119,122–124] How the interactions of the ferroelectric and the dielectric influence the negative capacitance behavior in this devices that lack an interfacial metal is important to understand. This chapter presents experimental data from bottom-gated 2D NC-FETs without a metallic interfacial layer and investigates the effects of increasing ferroelectric and dielectric oxide thicknesses and of dielectric

material composition on the negative capacitance behavior of the device. The result is a 2D NC-FET that achieves sub-60 mV/dec switching over a small region of drain current for a range of ferroelectric and dielectric thicknesses, along with insightful evidence of the dependencies of key device metrics on the gate stack composition.

7.2 Experimental Details

7.2.1 2D NC-FETs With Varying Ferroelectric Thickness

Hafnium zirconium oxide was grown in a custom-built Kurt J. Lesker plasma-enhanced ALD (PE-ALD) cluster system using precursors tetrakis(dimethylamino)hafnium ($Hf(N(CH_3)_2)_4$) (TDMAH) heated to 85°C and tetrakis(dimethylamino)zirconium(IV) ($Zr(N(CH_3)_2)_4$) (TDMAZ) heated to 75°C on three separate wafers. Water vapor was used to form the oxides. The ALD chamber was set to 271°C and left for 60 minutes to stabilize at temperature. HZO films were grown in a 1:1 Hf:Zr ratio by alternating cycles of TDMAH, water vapor, TDMAZ, water vapor. The pulse/purge times of each were: 20 ms/10 s, 140 ms/10 s, 200 ms/20 s, 140 ms/10 s, respectively. The alternating cycles were repeated either 33 times for 6 nm, 66 times for 12 nm, or 99 times for 18 nm HZO film growth. Immediately afterward, hafnium oxide was deposited on each wafer with TDMAH at 85°C and water as the precursors. The pulse/purge times were 20 ms/10 s and 140 ms/10 s, respectively. The alternating cycles were repeated 100 times for 10 nm HfO_2 on each wafer.

7.2.2 2D NC-FETs With Varying Dielectric Thickness

All ALD films were grown using the same procedure described in Chapter 7.2.1, with the following exceptions. The alternating cycles of TDMAH/water/TDMAZ/water were repeated 66 times for 12 nm HZO film growth. Immediately afterward, hafnium oxide was deposited on each wafer with TDMAH at 85°C and water as the precursors. The alternating cycles were repeated either 50 times (for 5 nm), 100 times (for 10 nm), or 150 times (for 15 nm) HfO_2 on each wafer.

7.2.3 2D NC-FETs with Varying Dielectric Composition

ALD films were grown using the previously outlined procedure in Chapter 7.2.1, with the following exceptions. The alternating cycles were repeated either 22 times for 4 nm HZO film growth. Immediately afterward, a dielectric material of aluminum oxide, hafnium oxide, or zirconium oxide was deposited on each of the wafers. The TDMAH at 85°C, TMA at room temperature, TDMAZ at 75°C, and water were the precursors. The Al_2O_3 was grown by alternating cycles of trimethylaluminum (TMA) and water with pulse/purge times or 20 ms/10 s and 140 ms/10 s, respectively. HfO_2 was grown by alternating cycles of TDMAH and water with pulse/purge times or 20 ms/10 s and 140 ms/10 s, respectively. ZrO_2 was grown by alternating cycles of TDMAH and water with pulse/purge times or 250 ms/10 s and 140 ms/10 s, respectively. The alternating cycles were repeated 40 times for 4 nm dielectric oxide growth on each wafer.

7.2.4 2D NC-FET Device Fabrication

PMMA 950 A3 was spin- coated over the HfO_2 at 500 rpm for 5 s and 4000 rpm for 60 s, then baked at 180°C for 180 s. The alignment mark pattern was written using electron beam lithography (EBL) in a 600 μm field of view with 60,000 exposure points. The electron beam was set to a 2 nA current with an exposure of 0.45 μs to create a dose of ~1145 μC/cm2. The pattern was developed in a 3:1 ratio of IPA to MIBK for 120 s, rinsed with IPA, and dried with nitrogen gas. The alignment pattern was metallized using an electron beam evaporator with 5 nm Ti, 30 nm Au. Lift-off was performed in a beaker of acetone heated to 80°C for ~5 minutes. The wafer was rinsed with IPA and dried under nitrogen gas. MoS_2 was mechanically exfoliated over the patterned regions. MoS_2 flake thicknesses were optically characterized and confirmed with AFM, with flake thicknesses nominally chosen between ~3-5 nm for device fabrication. PMMA 950 A3 was spin-coated over the capacitors with MoS_2 at 500 rpm for 5 s and at 4000 rpm for 60 s, then baked at 180°C for 60 s. The same PMMA/EBL/development process previously described was employed to write the contacts and leads in the same step. Once written and developed, the contacts and leads were metallized with 25 nm Ni. Lift-off was performed in a beaker of acetone heated to 80°C for ~15 minutes. The wafer was rinsed with IPA and dried under nitrogen gas. The PMMA/EBL/development process was again repeated to create the S/D pads, followed by metallization using an electron beam evaporator with 2 nm Ti/15 nm Pd/20 nm Au. Lift-off was performed in a beaker of

acetone heated to 80°C for ~5 minutes. The 2D NC-FETs and the MoS_2 2D-FETs were characterized with an Agilent (Keysight Technologies) B1500A Semiconductor Parameter Analyzer.

7.2 Results and Discussion

The dependence of the 2D NC-FET operation on the gate dielectric and ferroelectric thicknesses were independently demonstrated and are displayed in Figure 34. The impact of a 10 nm HfO_2 gate oxide with either a 6, 12, or 18 nm HZO ferroelectric layer is shown in Fig. 34(a-c). The threshold voltages have a positive shift with increasing HZO thickness, from -7 V at 6 nm HZO to -2 V at 18 nm HZO. This is opposite what was observed in Chapter 6 when the devices included TiN interfacial layers and is explained through the variations in the device structure. First, the overlap capacitance of these devices is less than it was for those in Chapter 6. The devices in Chapter 6 were fabricated over a large TiN/HZO/TiN ferroelectric capacitor, which allowed the ferroelectric behavior to average over the entire area. Devices in this chapter had no interfacial layer, and therefore the overlap capacitance within the device was significantly reduced to only the active area. Second, the HZO capacitors within the device structure of Chapter 6 encompassed a larger area when compared to the present devices, meaning that the ferroelectric response played a larger role in device behavior in Chapter 6. Finally, and most substantially, the devices in Chapter 6 had both the HZO and the HfO_2 increase in thickness simultaneously and did not look into how each

thickness affected the device performance. As seen in Figure 34(d-f), the fabricated devices that maintained a 12 nm HZO ferroelectric layer while the HfO_2 layer was increased from 5 to 10 to 15 nm displayed a negative shift in the threshold voltages from -2 V at 5 nm to -7 V at 15 nm. Hence, there is an asymmetric scaling behavior for V_t between the ferroelectric and dielectric layer thicknesses. These results highlight the importance of careful gate stack design in order to realize low-voltage 2D NC-FET.

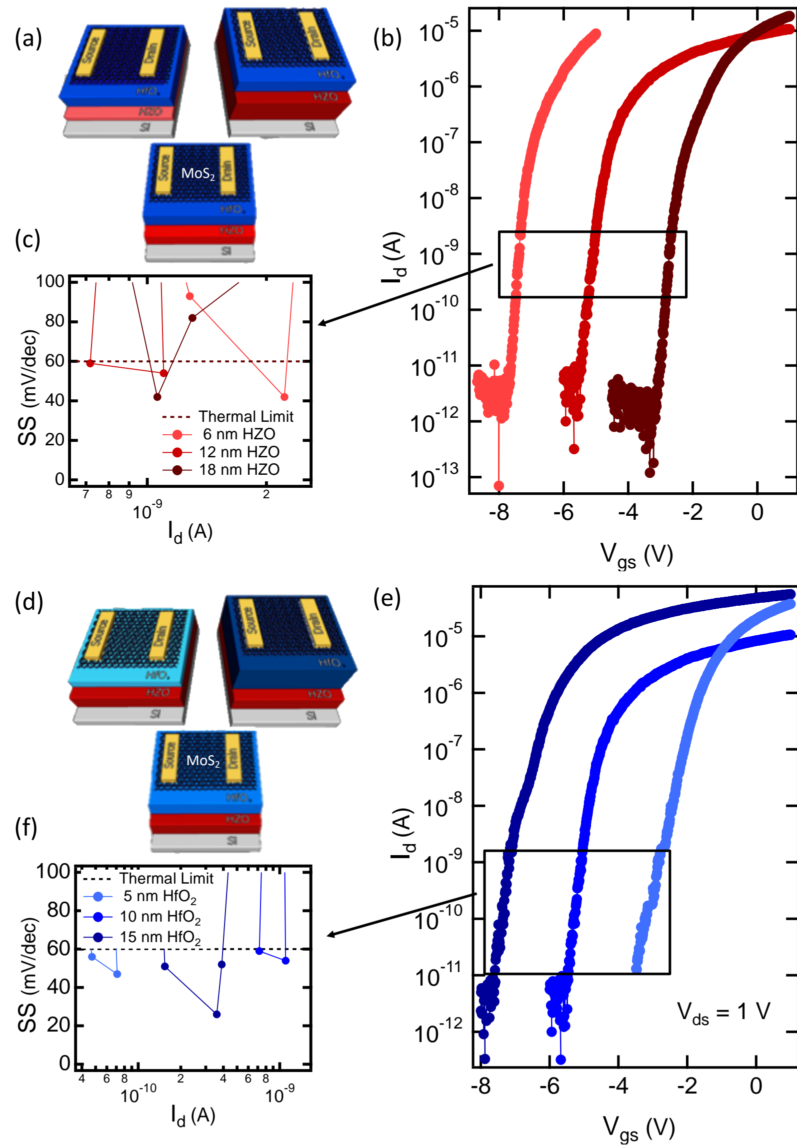

Figure 34. Impact of ferroelectric and dielectric thickness scaling on 2D NC-FETs. (a) Schematics of device structures detailing the increasing HZO thickness. (b) Subthreshold curves showing the positive threshold voltage shift, and (c) subthreshold swing (SS) from the region of sub-60 mV/dec behavior for the HZO thickness scaling devices (HfO_2 fixed at 10 nm). (d) Schematics, (e) Subthreshold curves for the HfO_2 thickness scaling devices (HZO fixed at 12 nm) and (f) SS.

It is also important to note that the most promising 2D NC-FET behavior appears to arise when the ferroelectric thickness matches the dielectric thickness. Due to this observation, 2D NC-FETs were then fabricated with equal ferroelectric and dielectric thicknesses of 4 nm each, using three different ALD-grown high-k dielectrics: zirconium oxide (zirconia, ZrO_2), hafnium oxide (hafnia, HfO_2), and aluminum oxide (alumina, Al_2O_3), the results of which are displayed in Figure 35.

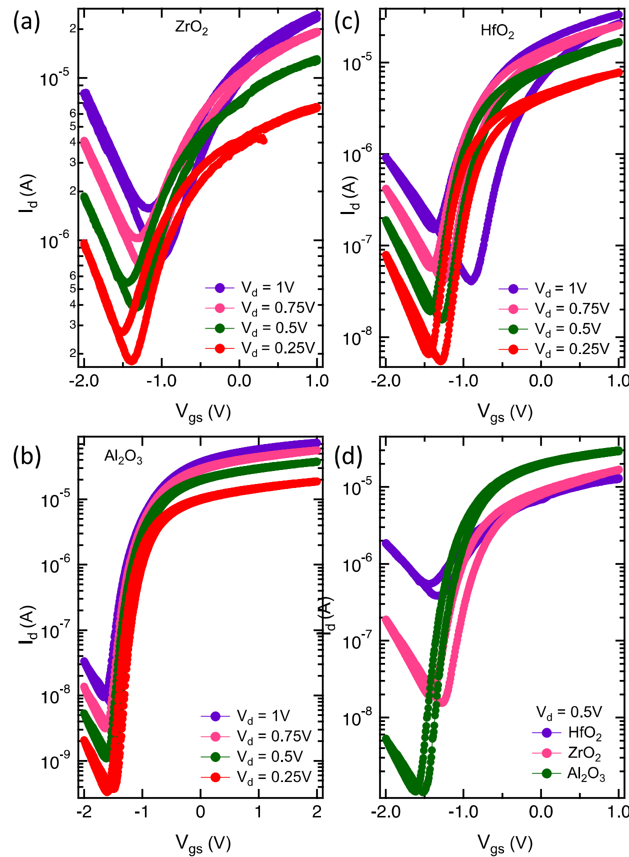

Figure 35. Impact of dielectric type on 2D NC-FET performance. Subthreshold curves for devices with (a) ZrO_2, (b) HfO_2, and (c) Al_2O_3 as the gate oxide at multiple drain biases. (d) Comparative curves for devices at V_{ds} = 0.5 V.

Each dielectric was selected for its large permittivity and ease of growth. The devices with hafnia and zirconia had a considerably small on-to-off-current ratio (I_{ON} : I_{OFF}) ratio of 1-2 orders of magnitude and tended to have larger gate leakage currents. This insufficient switching behavior is attributed to interfacial effects, such as interface traps, that occur between the dielectric and ferroelectric, as well as between the dielectric and MoS_2. The devices with alumina, however, had an I_{ON} : I_{OFF} of $\geq$ 4 orders of magnitude and significantly less leakage throughout the device.

In addition to the leakage, none of the 4 nm HZO devices were able to produce the steep switching behavior observed in previous 2D NC-FETs. This is a direct consequence of the reduced ferroelectric behavior of the HZO due to the presence of a passive layer at the interface between the ferroelectric and the dielectric layers that suppresses the spontaneous polarization.[125] The passive layer can arise when the ferroelectric is in a parallel plate capacitor configuration and there are variations in the out-of-place component of the effective permittivity. These variations then create a depolarization field previously described in Chapter 3.3.2. This is experimentally observed in Figure 36(c), where the passive layer suppressed the spontaneous polarization of the 4 nm HZO ferroelectric layer and thus stifled the negative capacitance effect, resulting in transistor switching above the thermal limit. The presence of a passive layer at the interface further explains minimal nonlinear polarization observed with the 6 nm HZO curve in Fig. 36(a) and with all curves in Figure 36(c).

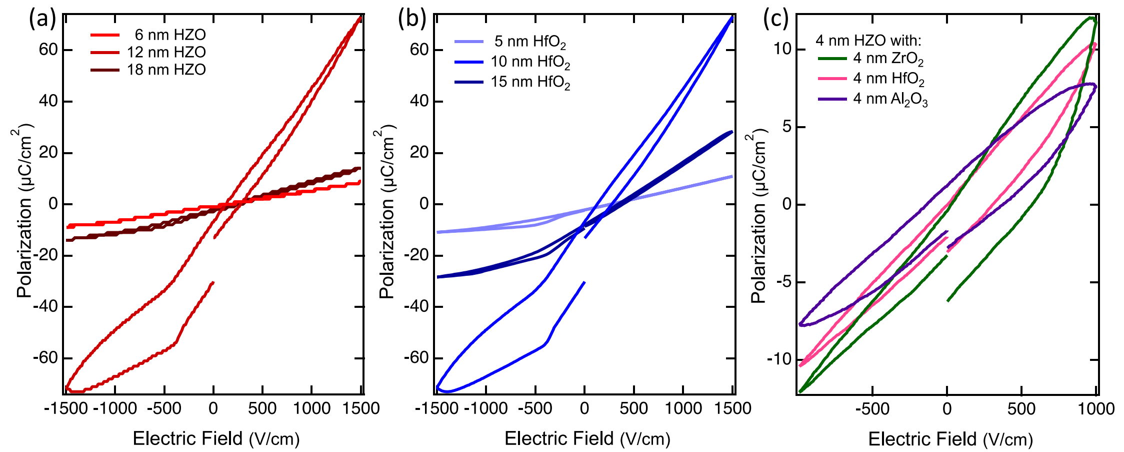

Figure 36. Polarization – electric field curves for devices with (a) increasing HZO layers, (b) increasing HfO_2 layers, and (c) the same HZO thickness with different dielectric materials. Thicker HZO layers have smaller ferroelectric responses, while the thinnest HZO had larger depolarization fields, leading to the largest polarization displayed in the 12 nm HZO. A similar argument can be made for the devices with increasing HfO_2 – thinner HfO_2 cannot sufficiently stabilize ferroelectric behavior, while the thickest HfO_2 overshadows the ferroelectric polarization. Therefore, the largest ferroelectric response arises from the devices with 10 nm HfO_2.

Finally, the performance of the 4 nm HZO/4 nm Al_2O_3 device was compared to that of the 2D NC-FET with 12 nm HZO/10 nm HfO_2 and TiN interfacial layers, shown in Fig. 37.

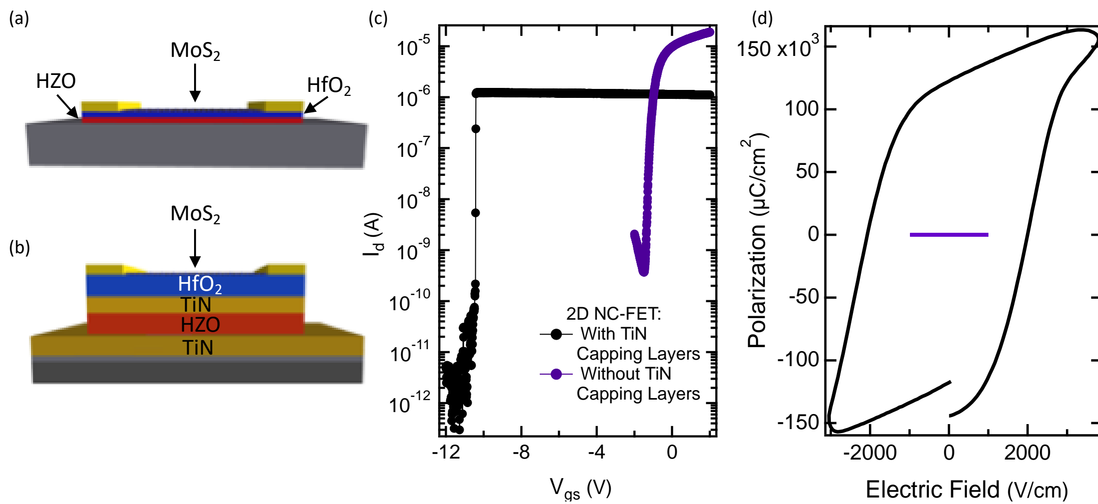

Figure 37. Impact of interfacial metal layer (TiN) in 2D NC-FET performance. (a) Schematic of the 2D NC-FET without (top) and with TiN (bottom) capping layers, (b) subthreshold curves displaying the dramatic difference in the threshold voltage and in the subthreshold swing, and (c) P-E curves for the same devices. The much larger nonlinear polarization of the 2D NC-FET with TiN capping layers contributes significantly to the presence of the negative capacitance effect.

Though both devices are of similar ferroelectric and dielectric thicknesses, the 10 nm HZO device has significantly improved subthreshold characteristics stemming from the inclusion of the TiN interfacial layers. The inclusion of the TiN interfacial layer between the ferroelectric and the dielectric in the gate stack was observed to boost the ferroelectric response of the HZO thin film for realizing a substantial sub-60 mV/dec switching region.

7.3 Conclusion

In conclusion, 2D NC-FETs without metallic interfacial layers were found to exhibit slight sub-60 mV/dec switching in multiple ferroelectric/dielectric thickness configurations. Thicker ferroelectric films resulted in a positive shift of the threshold voltage, while thicker dielectric layers caused the threshold voltage to shift negatively. The composition of the dielectric layer was found to have a large impact on the performance of the device, as FETs fabricated with HfO_2 or ZrO_2 as the dielectric displayed the largest I_{OFF} and smallest $^{ON}/_{OFF}$ current ratios. At a 4 nm HZO thickness, the passive layer at the interface impeded ferroelectricity and inhibited the negative capacitance effect. These results express the ability to achieve sub-60 mV/dec switching when the ferroelectric and dielectric layers are sufficient to overcome the depolarizing field and demonstrate the need for metallic interfacial layers to achieve sustained sub-60 mV/dec switching in 2D NC-FETs.

8. Conclusions and Recommendations

This dissertation has detailed the fabrication and integration of ferroelectric materials into the gate stack of top-gated and back-gated 2D-FETs. The ferroelectric material hafnium zirconium oxide has been shown to be CMOS process compatible and capable of achieving steep switching in a range of thicknesses. During development of these processes, many advantages of, and issues with, the 2D NC-FET were revealed. This chapter provides a summary of the advantages as well as recommendations for future research. Moderate familiarity with the work described in Chapters 5-7 is assumed here.

8.1 Conclusions

This work has brought significant progress to the field of low-voltage transistors, starting with the first experimental demonstration of the 2D NC-FET using polymeric ferroelectric P(VDF-TrFE) (Chapter 5). While the polymer was found to be unstable, this first 2D NC-FET yielded sub-60 mV/dec switching for several orders of magnitude in drain current. However, the P(VDF-TrFE)-based 2D NC-FET did not allow for detailed characterization and further progress required utilization of a more robust ferroelectric.

Transitioning from the top-gated configuration of the P(VDF-TrFE)-based 2D NC-FET, the next major milestone in this work was the successful demonstration of a back-gated 2D NC-FET with a CMOS-compatible, robust ferroelectric of thin film HZO (Chapter 6). These devices displayed repeatable, reliable sustained sub-60 mV/dec

switching over more than 4 orders of magnitude with a minimum SS of 6 mV/dec. Using this configuration, the hysteresis and minimum subthreshold swing were found to be dependent on the applied drain bias, with lower values of each occurring with larger drain biases. The threshold voltage of the 2D NC-FET was shown to be dependent on the thickness of the ferroelectric and dielectric layers, as when both were increased, the threshold voltage shifted negatively. Finally, the metallic interfacial layer between the ferroelectric and dielectric were shown to be of extreme importance in achieving sustained steep switching, as when these layers were removed in the 2D NC-FETs the subthreshold performance degraded substantially (Chapter 7). The interfacial layer was further found to reduce the depolarization field, thus increasing the ferroelectric response of the HZO and creating a larger NC effect.

At the onset of this work, in 2014, there were only a handful of published works reporting on NC-FETs, all of which involved the use of Si channels. Now, dozens of groups are actively studying these devices for their promising low-voltage operation, including a number of papers that integrate 2D channels with NC gate stacks. The pioneering work presented in this dissertation has influenced the field in ways that are already noticeable by providing experimental evidence for the capabilities of a 2D NC-FET. While considerable challenges remain for 2D NC-FETs, there's little doubt that progress in this field will continue and, as such, recommendations for future work are provided in the ensuing section.

8.2 Advantages, Issues, and Recommendations

The 2D NC-FET has the potential to revolutionize the semiconductor industry, yet there is still much work to be done. While completing these experiments, many advantages and integration issues have been revealed. Though these have been discussed herein, this section provides a review of the most pertinent challenges to provide a clearer perspective of the developments needed.

8.2.1 Interfacial Layer

The interfaces of the ferroelectric layer are crucial to maintaining ferroelectricity. Interfacial effects, such as interface traps can enlarge the depolarization field, reducing ferroelectric behavior. Further, for HZO, the capping effect of interfacial layers is important for driving the formation of the orthorhombic crystal phase, which is responsible for ferroelectricity. Hence, the addition of a metallic interfacial layer in 2D NC-FETs improved the interface and allowed for steep switching over a larger current range; however, it also introduced a parasitic overlap capacitance that deleteriously affected device performance.

Alternatives to the device fabrication in Chapters 5-7 include minimizing the overlap capacitance by removing the TiN/HZO/TiN capacitor from the entire substrate, except for immediately under the MoS_2 flake. One option to accomplish this is, after identifying the 2D flakes for devices, coat the wafer with a negative EBL resist and pattern it such that only the MoS_2 flakes will remain covered. After development, the

TiN/HZO/TiN capacitors can be etched with an inductively coupled-reactive ion etch (ICP-RIE). A layer of SiO_2 equal to the thickness of the TiN/HZO/TiN capacitor will need to be deposited to maintain device integrity and alleviate current leakage concerns. Source/drain contacts can then be fabricated as usual.

8.2.2 Threshold Voltage

Reducing the threshold voltage is key to reducing power consumption, especially for a steep-slope device like the 2D NC-FET. As expressed throughout this dissertation, understanding the interplay between the ferroelectric and dielectric layers is crucial to harnessing control over the threshold voltage. Chapter 6 provided an example of how the ferroelectric and the dielectric thicknesses negatively shift the threshold voltage when an interfacial layer is present. Chapter 7 detailed how the threshold voltage was independently controlled by the thickness of the ferroelectric or dielectric layers without an interfacial layer. Comparing these chapters indicates how the presence of the interfacial layer also influences the threshold voltage, making it crucial to more thoroughly investigate how each parameter affects the threshold voltage and how it can be scaled while maintaining steep switching.

One recommendation for doing so is to utilize the structure described in section 8.2.1 and independently alter the thickness of the ferroelectric layer, the dielectric layer, and the interfacial layer. This will provide a guide on how to appropriately scale the device to achieve a low-voltage, steep switching 2D NC-FET.

8.2.3 Dielectric Material

The choice of dielectric in the 2D NC-FET is essential for 2D NC-FET operation and steep switching. As shown in Chapter 7, the dielectric materials behave differently when integrated into the 2D NC-FET. It is therefore a recommendation that multiple dielectrics be considered and explored to incorporate into the 2D NC-FET, especially if considering a device that does not include an interfacial metal layer.

8.2.4 Switching Speed

Throughout this dissertation, there has been no mention of the potential issue of switching speed. This is because there is still much debate about whether NC-FETs will be able to switch at high frequencies or will be delayed by polarization times. Recent theoretical framework has shown that the intrinsic delay of doped-HfO_2 was at most 270 fs when the experimentally measured loss due to the inertia of the lattice atoms was included.[126] This delay is well below the required latency requirement of 10 ps for digital logic. While promising, experimental evidence of high frequency switching is absent from the current literature. It is highly recommended that the switching speed of 2D NC-FETs be thoroughly experimentally and theoretically investigated, perhaps using ring oscillators, prior to scaling up to manufacturing.

8.2.5 Manufacturing

Currently, the 2D NC-FET is not scalable to manufacturing, owing to the methods of 2D material placement, thickness determination, and source/drain contact

design. To achieve manufacturability, the 2D materials of known thicknesses would need to be easily placed in precise locations across a wafer. One recommendation to accomplish this is to explore large-area chemical vapor deposition (CVD) grown 2D materials as the thickness is more easily controlled.[70,127–132] The large area coverage reduces the need for precise placement, as after deposition, the 2D material could be patterned and etched, thus reducing the variability from device to device and dramatically increasing the yield of 2D NC-FETs per chip. Overall, the processes developed in this dissertation are applicable to a variety of 2D NC-FET configurations, though much more research is needed before the devices can be introduced to market.

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Biography

Felicia A. McGuire was born in Voorhees, NJ on January 25, 1990. She soon afterwards travelled to Birmingham, AL, where she spent her childhood and adolescence. Felicia was a competitive swimmer – her specialty was the 1500 m. She started college in 2008, immediately after graduating high school. Felicia attended the University of Denver for a year, then transferred to Sweet Briar College. Here she was given the honor of joining Iota Sigma Pi and Phi Beta Kappa. She graduated Cum Laude in 2012, with a B.S. in physics and in chemistry.

Felicia started graduate school at Duke University in 2012 under Dr. David Smith, working on plasmonics. It was here that she was a co-author on three papers, listed below. In 2014, Felicia was awarded both the National Science Foundation Graduate Research Fellowship and the National Defense Science and Engineering Graduate Fellowship. She then transferred to Dr. Aaron Franklin's group, where she authored and co-authored numerous more publications and presented at multiple conferences, all listed below.

Honors and Awards:

- National Science Foundation Graduate Research Fellowship (Awarded 2014, Accepted)
- National Defense Science and Engineering Graduate Fellowship (Awarded 2014, Declined)
- Iota Sigma Pi (National Honor Society for Women in Chemistry, 2011)
- Phi Beta Kappa (National Honor Society, 2012)

Publications:

1. McGuire, F.A., Noyce, S., Williams, W., Cheng, Z., Andrews, J., and Franklin, A.D., 2018. *IEEE EDL*, submitted.

2. McGuire, F.A., Lin, Y.-C., Price, K., Rayner, G.B., Khandelwal, S., Salahuddin, S., and Franklin, A.D., 2017. *Nanoletters, 17(8), 4801-4806.*

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Conferences:

1. Oral Presentation: F. McGuire, Y.-C. Lin, B. Rayner, A. D. Franklin, *Device Research Society* (2017)

2. Oral Presentation: F. Mcguire, Z. Cheng, A.D. Franklin. *Materials Research Society Fall Conference* (2015).